THE CONTROL OF BORON AUTODOPING DURING DEVICE PROCESSING FOR P/P+ EPI-WAFERS WITH NO BACK-SURFACE OXIDE SEAL

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Many device and wafer manufacturers have considered the removal of the back-surface oxide seal (sometimes referred to as "low temperature oxide" or LTO) on P/P+ epi-wafers as a method of reducing the overall cost. Equally importantly, for 300mm wafer manufacture, the process flow includes a double side polishing step to improve wafer flatness and backside cleanliness. This process flow makes the addition of a subsequent back-side oxide seal for 300mm wafers very costly because the oxide must be processed without physically contacting the previously polished front surface. The reason for adding an oxide seal to P/P+ wafers is to prevent autodoping, which involves the transport of boron from the heavily doped P+ substrate to the more lightly doped epi-layer of the same and/or an adjacent wafer during heat-treatment. The removal of the back-surface oxide film has, therefore, led device makers to be extremely concerned about the possibility of autodoping even during today's low thermal budget processes. The aim of this paper is to understand the magnitude of boron autodoping for P/P+ wafers with no oxide backseal under a variety of process conditions.

Experimental:

The experimental procedure consisted of measuring the total boron diffused into an N-type wafer, which was placed in between P/P+ wafers with no oxide backseal, during various thermal cycles in both nitrogen and dry oxygen ambients. The reason for using an N-type wafer was to ensure that the background boron doping level was as low as possible to increase the measurement sensitivity. Measurements of the near surface boron concentration, $[B]_{NS}$, and carrier concentration versus depth were then performed on the N-type wafers using SIMS and Spreading Resistance Profile (SRP) measurements for a range of temperatures and times in pure oxygen and nitrogen

In a slight modification to the above experiment, oxide films ranging in thickness from 0-1500Å were grown on the N-type wafers to determine the critical thickness of oxide required to prevent autodoping.

Results:

For anneals in N_2 in the temperature range 1050°C-1200 °C, the near surface [B] was found to be essentially independent of time for the range of anneal times studied (2-8 hours), but strongly dependent on temperature (Fig. 1). Under these conditions, $[B]_{NS}$ can be given by the expression $[B]_{NS} = 9.06 \times 10^{27} \exp(-3.25eV/kT)$ cm^{-3}. In contrast, no evidence of any boron could be detected by SIMS or SRP for any anneals in O_2 regardless of temperature or time (Fig. 1). Fig. 2 shows the results of the experiment to determine the critical oxide thickness required to prevent autodoping. **This critical thickness was found to be 600Å.** A separate experiment showed that if a furnace tube is loaded with boron during anneals of P/P+ wafers with no oxide backseal at high temperatures in N_2 gas, significant boron outgassing can occur during subsequent anneals.

In addition, autodoping of P/P+ wafers with no oxide backseal during the silicon wafer manufacturer's epitaxial deposition process can be minimized by a modification to the epi-reactor hardware/process.

Conclusions:

1) Boron autodoping was observed during anneals of P/P+ wafers with no oxide backseal during anneals in pure N_2 gas at high temperatures.
2) No autodoping could be detected for anneals in O_2 gas.
3) The critical oxide thickness on the wafer front surface required to prevent autodoping in a device process is 600Å, which is normally achieved during the initial stages of the device process.

In summary, boron autodoping for P/P+ wafers with no oxide backseal can be avoided in the device process by avoiding high temperature anneals in N_2 gas or by ensuring that wafers have a minimum oxide thickness of 600Å

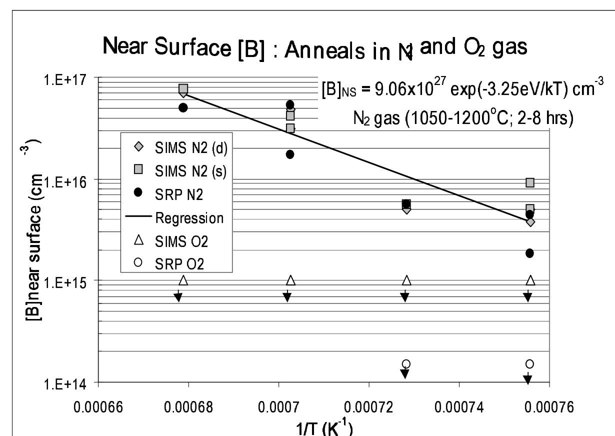

Figure 1 Summary of all $[B]_{NS}$ measurements extracted from SIMS (deep (d) and shallow (s)) profiles and SRP measurements for samples annealed in N_2 and O_2 gas as a function of temperature

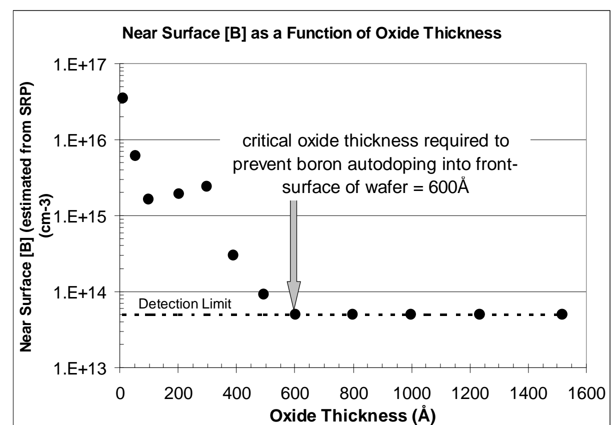

Figure 2 Estimated values of near surface boron concentration, $[B]_{NS}$, as a function of oxide thickness. Critical thickness of oxide needed to prevent boron autodoping into wafer front surface is ~600Å