Invention of Stacked Capacitor DRAM Cell

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One transistor type memory cell with planar capacitor structure (planar capacitor cell) had been employed in 4Kbit DRAM in mid 1970. I had investigated the issues of this planar capacitor cell from 1975 to 1976 and then I found that in the planar capacitor cell it is difficult to scale-down the memory cell size and the data stored in planar MOS capacitor are easily destroyed by collecting the minority carriers generated in the silicon substrate. In order to solve these problems, I proposed to stack the storage capacitor on the gate of switching transistor. We can achieve the larger capacitance in the smaller cell area and furthermore minimize the influences of minority carriers generated in the silicon substrate by stacking the storage capacitor on the gate of switching transistor. I called this new memory cell a Stacked Capacitor cell (STC). I submitted US patent of STC cell as shown in Fig.1 [1] and succeeded in fabricating a DRAM test chip with STC cell as shown in Fig.2 in 1977 [2][3]. In this test chip, I employed oxidized silicon nitride (ON) film and Ta2O5 film as a capacitor insulator for the first time. The current – electric filed characteristics of this capacitor insulator are shown in Fig.3. I found that the leakage current flowing through the silicon nitride film is dramatically reduced by oxidizing the surface and this led to use the O/N stacked film as the capacitor insulator. This ON stacked film was used in the 256Kbit DRAM with planar capacitor cell for the first time and then has been widely used in a higher density DRAM so far. However, in Ta2O5 film, I encountered the problem that the leakage current through the film significantly increases after high temperature processes. To solve this problem, I proposed to fabricate the storage capacitor with Ta2O5 film after the formation of bit line in 1980 [4]. In this STC cell with a modified structure, the storage capacitor is stacked on both the gate of switching transistor and the bit line. I called this STC cell a top capacitor type STC cell. This cell has been widely known with the name of Capacitance-Over-Bit line (COB) cell. The COB cell with Ta2O5 capacitor insulator has been employed in 64Mbit DRAM. After 16Mbit DRAM, STC cell structure has evolved employing the more complicated three-dimensional (3D) capacitor structure as shown in Fig.4. Recently, prototype 4Gbit DRAM has been fabricated using the cylindrical stacked capacitor cell with Ta2O5 capacitor insulator. Furthermore, high k materials such as BST, SBT and so forth are going to be used as the capacitor insulator to increase the storage capacitance.

References: [1]M. Koyanagi et al., US patent 4,151,607 (Filed Jul. 5, 1977, Patented Apr. 24, 1979), [2]M. Koyanagi et al., IEDM, pp.348-351 (1978), [3]M. Koyanagi et al., Jpn. J. Apply. Phys., pp.35-42 (1979), [4]M. Koyanagi et al., IEEE Trans. on Electron Devices, pp.1596-1601 (1980)

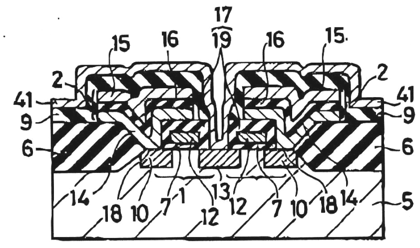

Fig.1 Cross-sectional structure of STC cell (USP 4,151,607)

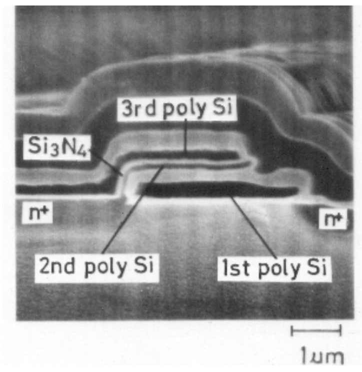

Fig.2 SEM cross section of STC cell

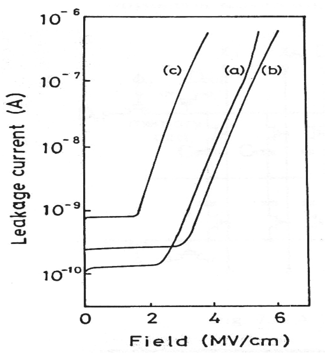

Fig.3 Leakage current – applied electric field characteristics of poly-Si –insulator– poly-Si capacitor structure. (a) poly-Si –SiO2– poly-Si (b) poly-Si – SiO2/Si3N4 (ON) – poly-Si (c) poly-Si /Ta– Ta2O5 – poly-Si

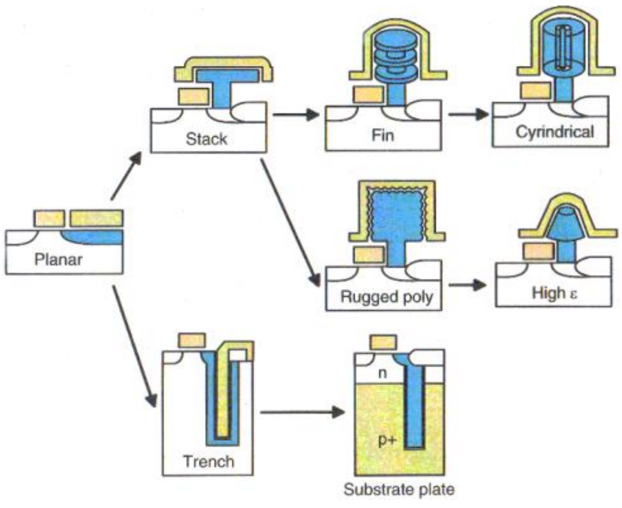

Fig.4 DRAM memory cell evolution