THE HIGH K CHALLENGES IN CMOS

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High K materials and requirements

The high K challenges in CMOS process integration are the topic of this paper. The needs of the industry are reviewed in terms of timing and performance. The choice of material has narrowed down to Hafnia and its silicates and aluminates. The properties of Hafnia-aluminate are given in figure 1.

Selected High K materials Fig 1	Properties (estimated)	
HfO_2-Al_2O_3 mixed oxide	K-value	15
	Thermo. Stable	(ΔG 230 kcal/mol)
	Amorphous	up to 1000 C
	Band-offset n	1.5 eV
	Band-offset p	3.5 eV

A tentative listing of specific requirements for High Performance and Low Power applications is given in figure 2.

Low leakage and manufacturability

For application in the field of portable equipment (mobile phones, palm-top etc) gate leakage in excess of the off current is unacceptable.
For high performance applications (such as desktop computers) stand–by power consumption is less of an issue. However, power dissipation might become critical above 10 A/cm^2. Manufacturability is thought to be the main drive for high K in high performance applications though.
By the year 2008 the high K solution for high performance is inevitable to realise sub nm gates. That same year low leakage applications will outgrow standard gate solutions because of the leakage current requirements. The roadmap is indicated in figure 3.

Metal gates

Thin metal layer with poly might be a first metal gate generation. This will solve the depletion problem but does not tackle the resistivity limitation of the poly gate. Full metal gate integration can be a final stage of metal gate integration into CMOS. This roadmap is depicted in figure 4.

SOC compatibility; cleaning strategy

SOC processing limits High K pre deposition clean and surface preparation strategies. Best, HF cleans should be avoided and because of this a chemical oxide starting surface is preferred. Chemical oxide starting surfaces match with low leakage high K solutions, but scaling of these chemical oxides will be required.

High K gate requirements (not ITRS)

	Low leakage	High performance
performance	Standby Current	High Speed
application	Analog/Digital	Digital
requirements	Low gate leakage	Heat dissipation
	Low noise	Reliability
year	2006	2008
Gate EOT	1.5(1.0) nm	1.0 (0.5) nm
voltage	1.2	0.8
leakage	0.1(1) A/cm^2	1(100) A/cm^2
material	Amorphous	
mobility	High	?
	low high field	only high field
clean	chemical/thermal (RTO) oxide	HF
process	?	Cluster tool

Figure 2 gate requirements

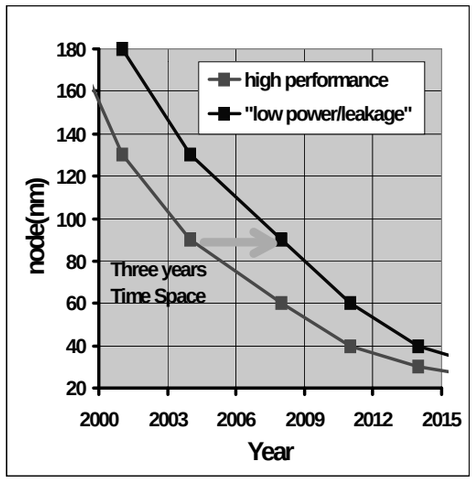

Figure 3 Two Roadmaps

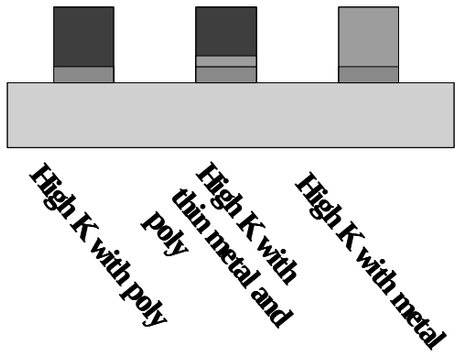

Figure 4 metal gate roadmap

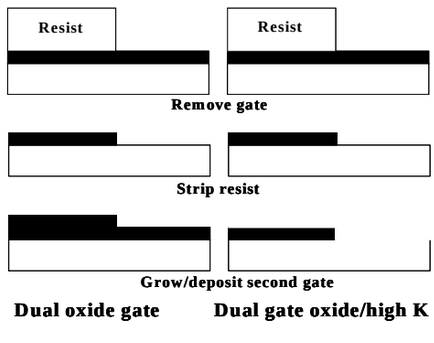

Figure 5 SOC with High K