Effective Intrinsic Gettering of Copper during a sub-quarter micron CMOS Process

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The importance of gettering of metallic impurities in silicon has widely recognized in the ULSI production. Metals such as Fe, Ni and Cu degrade critical performance of devices such as gate oxide integration (GOI) and junction leakage currents if they are precipitated in the proximity of the active device components. Copper, in particular draws high attention due to its unique behavior tending to diffuse fast and out-diffuse from the bulk and precipitate at surface. Although intrinsic gettering IG have been studied intensely over the years, its incorporation into the ULSI process is limited to a minimal level. This is mainly due to the concern about the thermal budget increase as traditional IG requires anneals the wafers for several hours at both high and low temperatures to form a sufficiently deep precipitate-free (or denuded) zone and a sufficiently high density of precipitates beneath this zone. The rapid progress in the device geometry shrinkage, which defaults device fabs to be more sensitive to metals as a rule, has recently brought up significantly revived interest in IG capabilities of silicon wafer substrates. Device fabs desire a reliable and robust IG technique with minimal side effects that would work well with low thermal budget processing. In this paper, we report that copper was successfully gettered by a specialty engineered IG technique, preventing it from forming a device-killing defect which had lowered the yield of a sub-quarter micron DRAM.

Prime grade 200mm diameter, p-type polished wafers were used, with the surface oriented 4^o off (100) and with the resistivity in the range of 9-12 ohm-cm. The initial oxygen concentration was in the range of 11.3-14.5 ppma in new ASTM.

In the particle count map, a high density of surface defects distributed in a ring pattern after a polysilicon gate process. The defect was imaged fibrous in SEM. From the previous study, copper was typically detected from the fibrous defect with a similar morphology by EDXS. In the surface metal analysis before and after gate oxidation, copper was found to increase to 5E11 at./cm^2 that is two orders of magnitude higher than before gate oxidation. From these results, the cause of the fibrous defect formation was copper contamination, as a result of either out-diffusion from the bulk of the starting wafer substrate or in-diffusion during the thermal gate oxidation.

In optical microscopy after Secco etching, the “good” wafer surface was imaged clean, whereas the “defective” wafer surface showed a high density of S-pits in the area where fibrous defects were found. S-pits are typically known to be an etching signature of metallic precipitates at the surface, especially caused by copper contamination when no gettering action takes place. In the cleaved cross-section, the sample without fibrous defects showed a high density of microdefects (BMDs), while the sample with S-pits did a low density of BMDs. This clearly demonstrates the correlation of S-pits with the IG activity that is indicated by the BMD density.

From these results, it is reasonable to believe that the fibrous defect was caused by copper precipitation due to the lack of IG. The copper containing precipitate served a nucleation site or a catalysis for fibrous substance during a LPCVD for polysilicon. The ring-pattern distribution of the fibrous defect can be explained with respect to the inhomogeneous radial distribution of grown-in BMD nuclei, a characteristic of the vacancy-interstitial mixed type crystal used in this study. Details in the intrinsic point defect reactions and oxygen behavior in the silicon crystal growth can be found elsewhere [1].

In the present study, we especially chose MDZ® applied as an IG solution [2]. During the MDZ® process, a vacancy profile template is created by means of rapid thermal processing (RTP) in the wafer after crystal growth. The resulting vacancy profile is quickly converted to the oxygen cluster depth distribution upon an initial heat treatment. This programmed cluster distribution then simply grows into larger precipitates upon further heat treatment. To demonstrate the effectiveness of gettering of copper, samples including the MDZ® treated wafer was subject to a DRAM thermal simulation following an intentional contamination with copper and the haze on the surface was evaluated. After an oxidation at 1100^oC for 80 min, haze was measured as an indicator of the effectiveness of gettering of the contaminated copper.

The control sample without any gettering treatment resulted in the ring-patterned haze, similarly to the fibrous defect distribution. Likewise, the sample with soft backside damage resulted in the ring-patterned haze indicative of ineffective gettering activity. Soft damage must have relaxed during the high temperature pre-gate thermal cycle in nitrogen ambient that does not supply interstitials high enough to form oxidation induced stacking faults (OSF) that are supposed to act pre-dominant gettering sites. In contrast, the MDZ® treated sample resulted in complete gettering, as evidenced by no haze formation on the surface. The cross-section of the MDZ® treated wafer showed a typically consistent BMD depth profile as typically reported elsewhere [3]. This result clearly demonstrates the effectiveness of MDZ® treated wafer for gettering copper in an advanced DRAM process.

In Summary, a device yield killing fibrous defect was formed by copper contamination in a sub-quarter micron CMOS process. The fibrous defect formation is correlated with the BMD density. It is demonstrated that MDZ® treated wafers provide an effective IG to getter copper.

References:

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