SINGLE-ELECTRON AND NANOSCOPIC DEVICE EVOLUTION

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Starting with possible end-of-roadmap CMOS-devices as a reference, an overview on single-electron devices (SET) will be given, with particular emphasis on basic principles and problems of room temperature device operation. It is commonly believed that scaling of CMOS-devices will technically persists down to gate length of 10 nm. Every other future possible device has to be compared with the properties of such a Nano-MOSFET. This nano- scale devices have to display a high on to off-current ratio (¿10E5, 1mA/m), exponential gate-characteristics and, if possible, a complementary device in order to realize normally on and off devices. As it will be shown, the size-dependent on-resistance and noise of single- electron transistors are a key obstacle for future implementation of these devices. For room temperature operation structure sizes smaller than 2 nm in diameter have to be achieved to yield sufficiently small capacitances for Coulomb blockade. This, in turn, limits the conductance of such devices to very low values mainly due to the limited tunnel area. Therefore, low working frequencies (¡ 10 MHz) for SET-devices are expected. A second factor affecting the high speed performance of a SET are time-dependent current fluctuations, which can be explained by the energy fluctuations of excited states in a quantum dot. As a consequence of these considerations, nanoscale devices based on tunneling and conduction through molecular structures will be proposed for sub-10-nm devices and discussed in terms of atomic-scale engineering.