OPTICAL INTERCONNECTS TO SILICON CMOS USING DENSELY-INTEGRATED OPTOELECTRONICS

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Silicon CMOS performance has improved steadily for more than 30 years because of the reduction in feature sizes of integrated circuits. While the physics governing the transistor favors this size reduction, the performance of the wires used for electrical interconnects does not improve significantly with this type of scaling. A new approach to signaling and clock distribution will be needed to take CMOS circuit performance beyond the limits imposed by electrical interconnects. Optical interconnects have the potential to circumvent these limitations and will likely be used for communications between future CMOS circuits, provided a number of technological issues can be addressed.

Many of the major problems with electrical interconnects, particularly those of low capacity and density, timing uncertainty, and high power dissipation are already beginning to limit the performance attainable by silicon electronics. To date, electrical interconnect performance has been enhanced by changing the technology used to fabricate the wiring layers on silicon chips. However, analysis of the physics governing the issues illustrates that the ultimate limitations have physical, not technological, origins. These limits are rapidly approaching (1), and their implications for future silicon CMOS circuits will be discussed in this talk.

Optical interconnects are the most promising candidate to solve the limitations imposed by electrical wiring, both for off-chip, and, possibly, for on-chip applications. This talk will address the ways in which optics can remove or minimize the problems already discussed, and how optics can offer features that were previously impossible with an electrical approach. Figure 1 shows a simplified schematic of a typical free-space chip-to-chip optical approach; it enables a much higher interconnect density and data rate than can be achieved using standard electrical techniques.

For optics to be considered a practical solution for the silicon microelectronics industry, the approaches taken in existing optical networks must be radically altered. Factors such as bandwidth density, power, and cost necessitate an approach that easily integrates large, two-dimensional arrays of small, low-capacitance optoelectronic devices with conventionally-processed silicon CMOS chips. Optoelectronic devices suitable for interconnect applications must generally allow surface-normal operation, and include p-i-n photodiodes and MSM photodetectors as input devices, and VCSELs and quantum-well modulators for optical outputs. The characteristics of these devices, as well as appropriate techniques for their integration (e.g., flip-chip bonding), will be discussed. Figure 2 shows an array of quantum-well modulators, both before and after flip-chip bonding to a silicon chip. The integration of passive optical components and the ways it can ease packaging issues will also be briefly addressed.

Finally, several experimentally-demonstrated systems will be described, including recent work on high-speed, multi-channel chip-to-chip optical links. Novel approaches that can improve link performance or add system functionality will also be presented. These approaches include optical clock distribution, the use of modelocked lasers to enhance timing (2) and reduce power requirements, and the demonstration of wavelength-division multiplexed optical interconnects (3).

References

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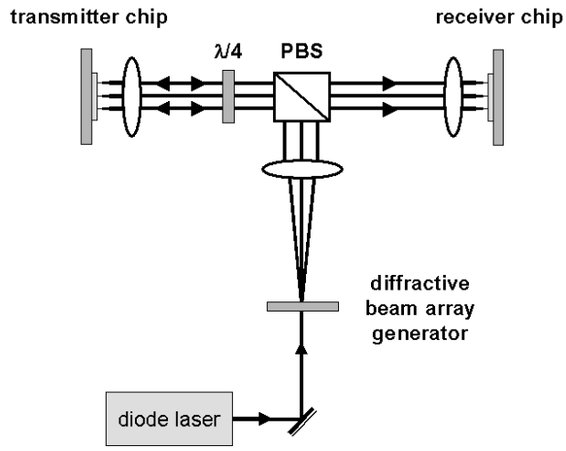
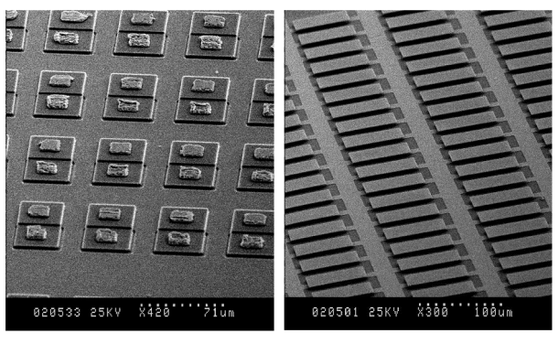


Figure 1. Schematic of a free-space chip-to-chip optical interconnect system that can allow thousands of high-frequency channels between two silicon CMOS integrated circuits. It employs surface-normal reflective modulators and photodiodes integrated on the silicon chips, and uses bulk optics for beam imaging. Polarizing optics can be used to reduce system losses.



(a) (b)

Figure 2. Scanning-electron micrograph of a quantum-well modulator array (a) before flip-chip bonding, and (b) following integration and GaAs substrate removal.