Integration of Millimeter-wave Photonics on Si

Hiromu Ishii
NTT Telecommunications Energy Laboratories
3-1 Morinosato Wakamiya, Atsugi,
Kanagawa 243-0198, Japan

Si technology has attracted a great deal of interest because of its possible use in implementing new functions on a chip by combining Si devices with sensors, RF devices, microelectromechanical systems (MEMS), and millimeter-wave (MMW) photonic devices. However, from the viewpoint of device features, recent ULSI processes aimed at submicron feature are not necessarily suitable for fabricating such new larger devices because of a technology gap in the 10-μm region [Fig. 1].[1-3] Therefore, we are developing **Sea**mless **i**ntegration **T**echnology (**SeaiT**) which fills this gap and enables us to seamlessly integrate Si devices with new functional ones.[1,3-8]

This paper details a combination of electronics and photonics: A prototype of an optical-to-electrical (OE) conversion module (from a 1.55-μm-wavelength light to MMW) with multilevel thick-gold damascene interconnections for MMW transmission lines used as coplanar waveguides (CPWs). The CPWs were integrated with a wafer-bonded uni-traveling carrier photodiode (UTC-PD)[9] on Si [Fig. 2].

Key issues for MMW transmission are reducing dielectric and conductor loss. For a low dielectric loss, transmission lines must be made far from Si substrates. Multilevel-interconnect technology using the damascene process is effective in making these transmission lines. For low conductor loss, gold is one of the best possible materials because of its low resistance and chemical stability. However, gold's chemical stability prevents a high-removal rate in chemical mechanical planarization (CMP), even though this high-removal rate is important in the practical damascene process. To achieve low-loss MMW transmission lines separated far from the Si in the OE conversion module, we used a positive-photosensitive organic polymer for the thick interlayer dielectrics. The photosensitive nature of the polymer allows us to make interconnection patterns and interlayer dielectrics simultaneously. We also succeeded in boosting the removal rate of thick-electroplated gold in CMP by simply adding H_2O_2 to conventional KIO_3-based alumina slurry. We clarified the mechanism for increasing in the removal rate of gold CMP as an I_2/IO_3^--based catalytic decomposition reaction of H_2O_2. These enable us to create a multilevel thick-gold damascene structure.

Figures 3(a) and (b) respectively show a top view and a cross-sectional image of the fabricated device. The CPWs are separated far from the Si substrate by thick interlayer dielectrics. The CPWs have a flat interface at each layer, showing the planarization of gold is perfect. Using an electro-optic sampling (EOS) technique,[10] we tested the transmission characteristics of >100-GHz MMW generated from a wafer-bonded UTC-PD that was back-illuminated by an ultrashort pulse laser [Fig. 2] and confirmed that the gold CPW with the multilevel damascene structure provides low effective permittivity and low dispersion.

In summary, we have fabricated a proto type of an OE conversion module composed of a thick-gold multilevel damascene interconnection as a CPW integrated with UTC-PD on Si. We did this by developing thick-polymer processes and a H_2O_2-added CMP of gold. EOS confirmed their effectiveness for a MMW transmission. Our SeaiT paves the way for fusing silicon devices with other new functions.

References

(1) H. Ishii et al., Proc. SPIE **4230**, 43 (2000).
(2) T. Sakurai, JSAP Int'l **3**, 15 (2001).
(3) H. Ishii et al., Proc. SPIE **4557**, 210 (2001).
(4) K. Saito et al., Proc. IEEE IITC 2000, p. 123, (2000).
(5) K. Machida et al., Tech. Dig. IEEE IEDM 1999, p. 887, (1999).
(6) N. Sato et al., Tech. Dig. IEEE IEDM 2001, p. 913, (2001).
(7) T. Minotani et al., Tech. Dig. IEEE MTT-S 2001, p. 57, (2001).
(8) A. Hirata et al., IEEE Trans. Microwave Theory Tech. **49**, 2157 (2001).
(9) Y. Royter et al., Proc. SPIE **3795**, 619 (1999).
(10) T. Nagatsuma, IEICE Trans. Electron. **E79-C**, 482 (1996).

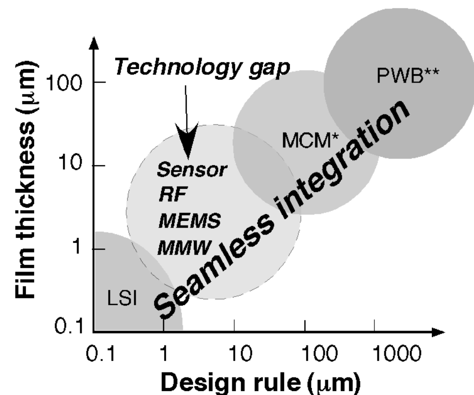

Fig. 1. Feature-based technology classification. *multi-chip module, **printed wired board

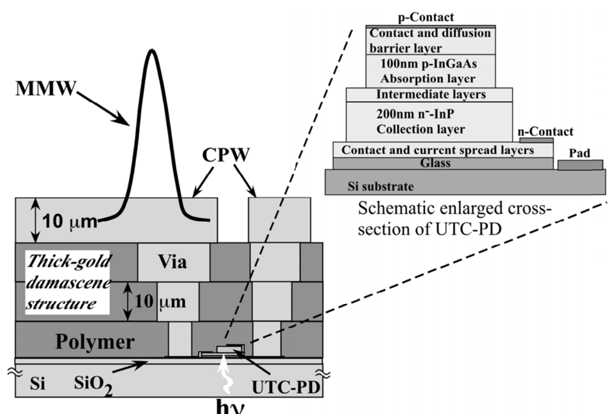

Fig. 2. Schematic cross-section of MMW-CPW integrated with UTC-PD on Si.

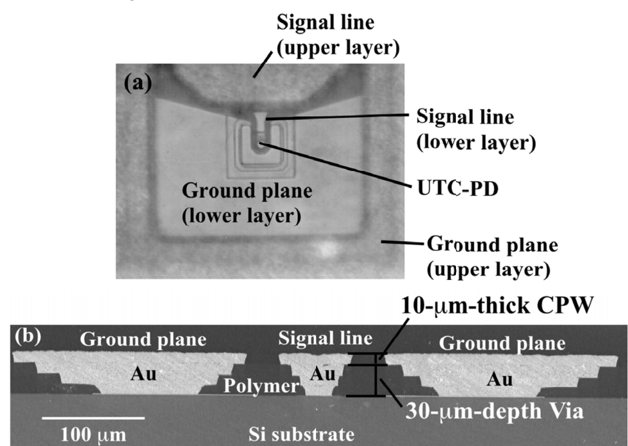

Fig. 3. Images of fabricated device: (a) Top view of the device, (b) cross-sectional SEM image of gold CPW fabricated far from Si substrate.