THE CASE FOR FIBER-TO-THE-PROCESSOR

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During the last decade (1990 – 2000), the combination of increased number of transistors, increased clock rate and improved architecture has dramatically enhanced total microprocessor performance. These trends have also dramatically increased power consumption and exerted significant bandwidth performance demands at the platform level.

In the coming years, the imbalance between microprocessor performance and memory access will be driven to a crisis point. As illustrated in Figure 1, with successive generations, the difference between microprocessor and memory-bus clock rate continues to grow. Without a new approach, the microprocessor will lose hundreds of process cycles while waiting for a single read from main memory.

The required performance cannot be achieved using a conventional all-electronic approach. At high memory-bus frequencies controlled impedance lines are required for electrical interconnects and this results in increased electrical power consumption. Another issue, intimately related to cost-effective packaging, is the difficulty in launching high-speed electrical signals. Controlled launch for each signal across a wide bus and maintaining impedance through vias is a major challenge for an all-electronic approach. In addition, electrical cross-talk and radiation from a bus operating at GHz rates makes it difficult to maintain signal integrity at the platform level.

The adoption of new photonic interconnect technology is the paradigm shift which can provide low-power, low latency, high-bandwidth data-delivery direct to the processor in future systems. It is the remarkable bandwidth density scaling, the use of power-efficient vertical-cavity surface-emitting lasers (VCSELs), low-cost interface electronics, and inexpensive packaging that make optical interconnects so attractive for addressing the needs of microprocessor platforms. The advantages are reduced power dissipation from high-speed chip IO, improved edge-connection density bandwidth, low cross-talk and zero EMI, and high-bandwidth to key resources such as main-memory and the system area network (SAN). The same high-bandwidth allows scaling to larger distributed multi-processor systems.

Incorporating the advantages of optical-interconnects with the integration capability of scaled CMOS electronics leads to a new FTTP design-point we call the encapsulated processor. The particular encapsulated processor concept shown schematically in Figure 2 is a single CMOS chip with fiber-optic ports as the only means of external high-speed data communication. There is a short low-power electrical link from the processor IC to the optical port IC embedded in the processor socket shown in Figure 3. Such FTTP-enabled systems require integration of 40 GB/s (320 Gb/s) VCSEL-based optical ports with high-performance CMOS processors.

The case for FTTP is a compelling one. In fact, it is inevitable that, just as fiber-optics migrated from WAN to LAN and then to SAN, it will be embraced as the enabling technology to propel microprocessor platforms to the next level of performance. There are just too many good reasons for adopting the technology.

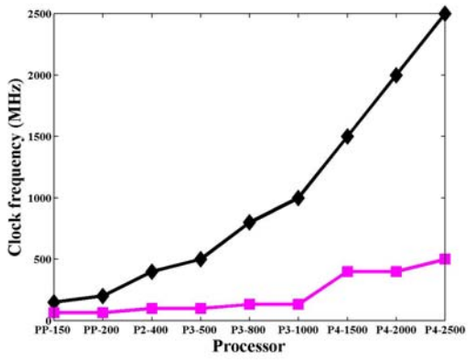

Figure 1 – The imbalance between microprocessor clock rate and memory bus clock rates continue to grow with successive generations of microprocessor.

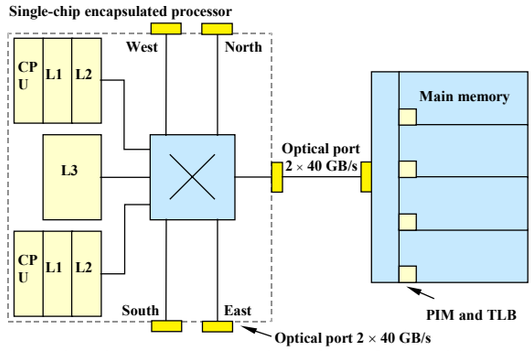

Figure 2 –The processor consists of two CPUs with L1 and L2 cache connected by a crossbar switch. The crossbar connects to on-chip L3 cache and multiple high-speed fiber-optic ports. Each fiber-optic port is capable of sustaining 40 GB/s (320 Gb/s) data throughput in each direction and one such port is dedicated to local main memory. Main memory could be configured to have its own processors and TLB. The remaining optical ports are available for IO and scalable SAN interconnect.

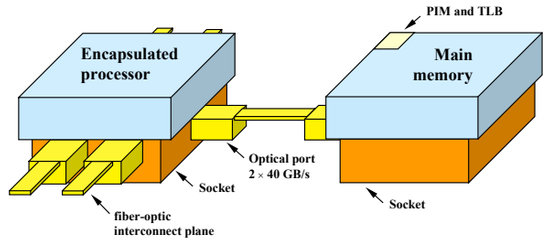

Figure 3 – The encapsulated processor includes a socket that supplies DC current and ground. Incorporated into the socket are the physical optical ports, each of which provide 2 × 40 GB/s data bandwidth external to the encapsulated processor. One optical port is dedicated to local main memory.