Integrated Imaging Sensor Systems with CMOS Active Pixel Sensor Technology

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Low-power, low-cost, high performance and miniature imaging sensor systems are expected to be widely used in consumer electronics in the near future. However, while CMOS technology has been responsible for the phenomenal growth in consumer electronics, till recently, the video technology remained outside this mainstream. Over the years, the incumbent technology in electronic imaging for consumer, commercial, and scientific applications has been charge-coupled devices (CCD).

The predominance of CCD in electronic imaging was due to its superior sensitivity, dynamic range, uniformity, low noise, and small pixel size. However, in order to achieve high (0.999999) charge transfer efficiency, CCDs require specialized silicon processing that is not compatible with CMOS technology. Furthermore, CCDs are high capacitance devices, requiring multiple non-standard and high voltage clocks and biases, while providing only serial output (no random access is provided). High device capacitance, large clock swing, need for DC-DC converters, and inability to integrate control amd processing.

Electronics on the imager chip make the CCD-based imaging system bulky and power-hungry (camcorder CCD power dissipation is around 10 W). Incompatibility with CMOS technology is a major barrier to realizing low-power, low-cost, digital, integrated system-on-a-chip using CCDs.

Despite several efforts in the decade of eighties and earlier, CMOS imaging performance lagged behind that of CCD. Availability of near or sub-micron CMOS technology, maturity of CMOS processing, in conjunction with the advent new low noise active pixel sensor (APS) concepts have altered the situation in the decade of the nineties [1, 2, 3]. APS approach enables high quality CMOS imagers with performance rivaling those of CCDs, drawing video technology into the mainstream of CMOS system-on-a-chip development.

The primary advantages of CMOS APS are low-cost, low-power (100-1000x lower than CCDs), simple digital interface, random access, simplicity of operation (single CMOS compatible power supply), high speed (>1000 frames per sec.), miniaturization (10-100x smaller) through system integration, and smartness by incorporating on-chip signal processing circuits. In this paper, we report the recent development of CMOS APS technology at Jet Propulsion Laboratory. We present the typical circuit design, operation, and performance of the CMOS APS, and the on-chip signal processing circuits for varies imaging system applications.

Figure 1 shows the microphotograph of a 5-wire (VDD, Ground, Clock, Digital-In, and Digital-Out) digital camera, Figure 2 shows the digital image captured with the on-chip imager. And, figure 3 shows the miniature digital one-chip camera.

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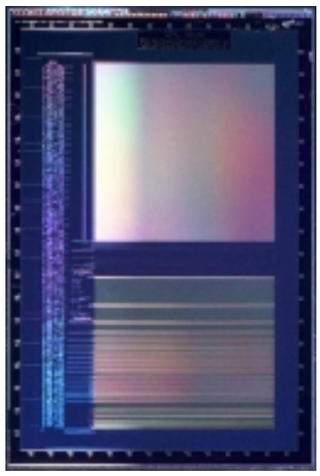

Fig. 1 Microphotograph of a 5-wire digital camera

Fig. 2 Digital image captured with the one-chip imager

Fig.3 Miniature digital one-chip camera