PFC Emissions Reduction and Process Improvements with Remote Plasma CVD Chamber Cleans

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The International Technology Roadmap for Semiconductors has identified Climate Change Mitigation as one of the five difficult Environment, Safety and Health (ESH) challenges through 2005 and beyond. This challenge specifically calls for reduction of emissions of high global warming potential chemicals, namely the perfluorocompounds used in semiconductor manufacturing. Towards addressing this challenge, the World Semiconductor Council (WSC), in April, 1999, established an international goal to reduce PFC emissions by 10% (absolute) of the 1995 baseline by 2010. In support of both the WSC goal and global ESH leadership, Motorola announced a more aggressive absolute reduction goal of 50% of the 1995 baseline. Because both semiconductor technology complexity and manufacturing capacity have dramatically increased since 1995, and will continue to do so toward 2010, Motorola anticipates that significant emissions reductions will be required to achieve this goal: 95% or greater from 200 mm films chamber clean and 90% or greater from high emitting 200 mm etch processes. After several years of evaluating various PFC emissions reduction technologies, only remote plasma chamber cleaning utilizing NF_3 has been demonstrated to be capable on 95% or greater PFC emissions reduction. [1]

In addition to PFC emissions reduction, remote plasma cleans with NF_3 provides potential for process benefits, such as reduced clean times (increased throughput potential), increased wafers processed between wet cleans, improved deposited film properties, and reduced chamber hardware consumables costs. These benefits have been demonstrated for both TEOS and silane-based films. Figure 1 presents the reduction in defects resulting from retrofitting CVD tools with remote plasma clean units.

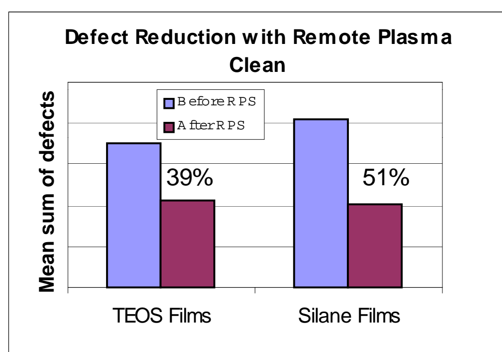

Figure 1 – Defect Reduction with Remote Plasma Clean

Because the utilization of NF_3 in the remote plasma cleaning processes is greater than 95%, and generally 99% or higher, the PFC emissions from chamber clean are virtually eliminated. Other NF_3-based chamber clean processes have similar utilization rates. For modern 200 mm fabs, the emissions contribution from chamber cleans can be 90% of the fab's total emissions. In 2000, the distribution of PFC emissions ranges from 50% films and 50% etch contribution to 95% films and 9% etch in Motorola 200 mm fabs. This ratio is highly dependent on the technology generation and product mix that the individual fab is running and can vary from year to year.

The goal that Motorola has established is a 50% absolute reduction in PFC emissions from the 1995 baseline by 2010. It is important to note that manufacturing capacity is greater and device complexity has increased dramatically since 1995. These increases are expected to continue through 2010 for the entire semiconductor industry. Figure 2 presents a projection of total PFC emissions from all existing fabs in 2005 compared to the 1995 baseline. The contributions of US fabs and non-US fabs are shown. In 2005, it is expected that all 200 mm fabs will have converted to NF_3-based chamber cleans. Some production expansion as well as older fab closures are incorporated into this projection.

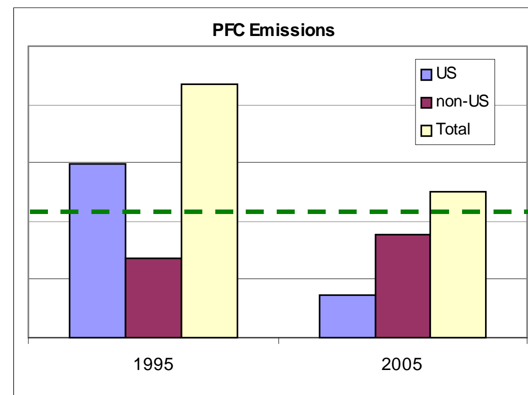

Figure 2 – Projected PFC Emissions Reduction

The emissions projection for 2005 accounts for conversion to NF_3-based cleans in 200 mm fabs only. No optimization activities are included for 150 mm fabs and no emissions reduction from etch processes have been included. Figure 1 shows that conversion to NF_3 cleans alone will almost achieve the 50% reduction goal. And, with some emissions reduction activity in non-200 mm fabs or some reduction in etch emissions, the 50% reduction goal could be achieved by 2005. This, of course, assumes no new contributions from etch processes in future capacity expansions or new fabs. Therefore, some level of emissions reduction activity will likely be required for high emitting etch processes. [2]

Remote plasma cleans have been demonstrated to be a viable option for PFC emissions reduction, achieving the reduction target of 95% or greater from CVD chamber cleans. Implementation of Remote Clean through installed base retrofitting and new tool purchases will result in significant PFC emissions reduction for a 200 mm fab, and would allow for significant progress towards a goal of 50% emissions reduction. Significant process benefits have also been achieved through remote plasma clean upgrades on both TEOS and silane based systems.

By implementing NF_3-based CVD chamber cleans, it is projected that a modern 200 mm fab could reduce PFC emissions to 1997 levels even with a 4X or greater net increase in PFC usage and proliferation of advanced technologies, such as multilevel metallization and low k dielectric films. By implementing NF_3-based cleans across all 200 mm fabs, it is possible to reduce overall PFC emissions nearly to the goal of 50% of the 1995 baseline. Thus, once the CVD chamber clean solutions have been implemented, the focus can turn to process optimization in older fabs and emission reduction in high emitting etch processes.

REFERENCES

[1] Mendicino, L., P.T. Brown, S. Filipiak, A. Atherton, M. Seamons, B. Thakur, H. Deshong, T. Vaughan, T. Nowak, D. Silvetti, "A Partnership for PFC Emissions Reduction," Semicon SW, October, 1999, p.D1-10.

[2] Mendicino, L., P.T. Brown, C. Nauert, S. Filipiak, H. Estep, M. Fletcher "A Partnership for PFC Emissions Reduction," Semicon SW, October, 2001.