Thermal Technologies for sub-100nm CMOS Scaling

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The increasing demands on device performance and manufacturing supply chain cost reductions, as driven by Moore's law, require important shifts in thermal technologies that arise from two primary issues: Technical roadblocks to device scaling require new process capability, and front end of line (FEOL) thermal processing plays a key role in fab cycle time and inventories. In particular, increasing development cost and time to market issues have put abundant focus on fast cycle time, reduced capital cost. The single wafer processing approach for front-end development and manufacturing will be highlighted.

This paper describes the latest film and product electrical device performance characterization for process and integration technologies that are required for CMOS scaling below 100nm. Particular emphasis is given to the critical challenges of equivalent oxide thickness (EOT) reductions for advanced logic integration. Optimization of V_{th}, I_{dsat}, and other parameters on product wafer structures will be shown for nitrided SiO_2 based gate stacks in the 10A to 13A range. These are correlated with *in-situ* plasma characterization, nitrogen profiling with PEELs and grazing incidence PES, and PES bonding characterization. These results will also be compared with ALD and MOCVD medium K and high K results. Thermal budget requirements have changed production technologies for ultra-low thermal budget RTCVD and ALD Nitride films and ultra-shallow junctions, which are discussed in terms of device impact.

Further improvements in the cost drivers of Moore's Law are demonstrated using a novel approach to modeling at the fab and supply chain levels that quantifies the incremental and collective impact on manufacturing and supply chain costs as a function of changes in tool configuration for each technology. As opposed to traditional cost models, this approach does not simply compare the device cost impact of simple tool throughput per capital cost dollar. For example, we take into account the fab operations cost impact, the fab inventory impact, the cost of capital impact, and the time to market revenue impact, to determine a supply chain Economic Value Add (EVA).