Manufacturability of SiGe:C Epitaxy for Heterojunction Bipolar Transistors integrated in a BiCMOS Technology

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We show excellent manufacturability of the SiGe:C epitaxy process based on growth characteristics and device data.

Introduction

The incorporation of low concentrations of carbon ($\leq 10^{20}$ cm^{-3}) into the SiGe region of a HBT can significantly suppress boron outdiffusion. We demonstrated that transistors with excellent static and dynamic parameters can be fabricated with epitaxial SiGe:C layers (1-4). The main result of these investigations was that carbon supersaturation can preserve steep doping profiles without degrading fundamental transistor parameters. In result, the RF performance can markedly be improved. Compared to SiGe technologies, the addition of carbon provides significantly greater flexibility in process design, offers wider latitude in process margins, and improved scalability of the transistor (2). Moreover a new modular SiGe:C BiCMOS integration scheme was shown introducing the HBTs before CMOS, which is possible using C containing SiGe base only (5).

SiGe:C Epitaxy

The SiGe:C base of the HBTs was deposited using a commercial, single wafer Reduced Pressure CVD (RPCVD) system. The C doping was performed in-situ during the SiGe deposition. For the suppression of B diffusion the C has to be incorporated substitutionally. Substitutional to interstitial ratio of C is determined by the growth conditions mainly. Fig. 1 shows the substitutional C measured by X-ray diffraction (XRD) and the total C concentration measured by SIMS for different C concentration levels as function of the deposition temperature. At low C level there is no significant difference between XRD and SIMS results and no remarkable impact of the deposition temperature. For high C concentration and with increasing temperature, the substitutional C concentration is decreasing.

Device Results

Various types of SiGe:C HBTs can simultaneously be fabricated in the BiCMOS process, covering a wide range in BV_{CEO} and f_T (6). Here, we present results from the qualified 0.25 µm BiCMOS process with HBTs featuring 3.2 V BV_{CEO}/ 60 GHz f_T and 2.5 V BV_{CEO}/ 80 GHz f_T. Figs. 2 – 4 show statistical data, obtained on 31 wafers taken from 7 lots. The data stem from 9 wafer sites. Fig. 2 shows an R_{SBi} histogram demonstrating the high reproducibility of the epitaxial HBT base doping regime. Fig. 3 proves high wafer yields of typically more than 90% for arrays with 4096 transistors in parallel. These yields take benefit from a very robust H_2 bake, carried out immediately before the epi process starts. Finally, high RF circuit performance with excellent reproducibility is demonstrated in Fig. 4, showing CML ring oscillator delay times with a mean value of 8.05 ps and σ of only 0.16 ps.

References

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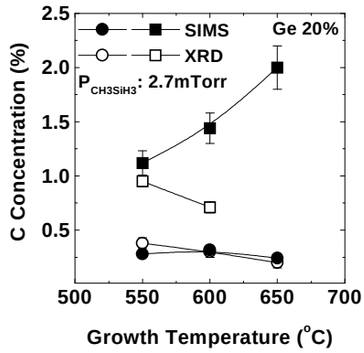

Fig.1: Substitutional (XRD) and total C (SIMS) concentration as function of the deposition temperature at low and high C concentration

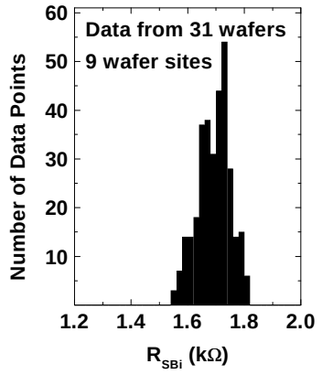

Fig.2: Histogram of HBT internal base sheet resistance (R_{SBi}).

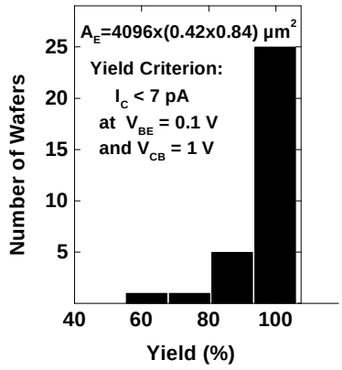

Fig.3: Histogram of wafer yield for arrays with 4096 high-BV_{CEO} HBTs in parallel.

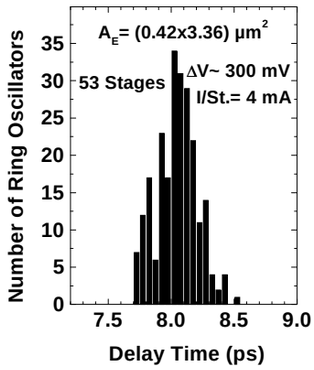

Fig.4: Histogram of CML ring oscillator delay times. For the ring oscillators, the high-f_T HBTs were used.