Microloading Effect in RTCVD Reactors

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Abstract

This report describes a microloading effect observed during rapid thermal chemical vapor deposition (RTCVD) of silicon nitride. We have found that a fast deposition rate makes an RTCVD reactor susceptible to microloading effects. The degree of microloading depends on the pattern density, aspect ratio, and relative size of microstructures. The thickness of SiN spacer in the middle of a dense and large memory array is found to be half of that of SiN spacer in a low-pattern-density region. The microloading effect is stronger for ICs based on smaller groundrules with increased level of system-level integration. In addition, the report discusses the physical origin of this and presents experimental data showing dependence of the microloading effect on the effective local surface area.

Usually, the term "Microloading Effect" is commonly used in the literature on Reactive Ion Etching (RIE) processes, where it refers to the etch rate dependence on the pattern density. By analogy with RIE, we define the deposition-based microloading effect as the growth rate dependence on the collection of microstructures. Contrary to RIE, the microloading effect depends not only on the pattern density but also on the aspect ratio. Fig. 1 schematically illustrates two semi-infinite adjacent microstructures with different pattern density and aspect ratio. The growth rate of SiN in a commercial RTCVD reactor is constant and different far from the border between the microstructures. In addition, the growth rate varies in the proximity of the border. The characteristic scale of the variation is of the order of several tens of microns and is different than that of the conformality or step-coverage effect.

Because of a relatively large area affected by microloading, the size of a microstructure array as well as the proximity of different arrays defines the degree of the effect. Fig. 2 shows a SiN spacer thickness variation as a function of the size of adjacent memory array. Figs. 2 (a) and (b) show gate structures of a relatively large and dense memory array and a low-pattern-density logic area adjacent to the array, respectively. Fig. 2 (c) shows the same gate structure as Fig. 2 (b) but adjacent to a smaller memory array. While the thickness of the spacers shown in Figs. 2 (a) and (b) is substantially the same, the spacer shown in Fig 2 (c) is almost twice the size. This is a clear evidence of the effect.

Fig. 3 demonstrates the dependence of the degree of microloading on the local surface area. The growth rate difference is given relative to the growth rate on a blanket wafer. The relative surface area is also referenced to a flat surface and represents an average surface area of a relatively large portion of a chip. The thickness of the spacer is 50% thinner in the dense memory array.

System-level integration is expected to play a major role in the future generations of ICs. Multiple microstructures of different size and smaller ground rules make the chip more susceptible to the microloading effect. RTCVD tools are also susceptible to the microloading due to the fast deposition rate. Accordingly, despite the thermal budget advantage, the microloading effect poses a serious obstacle for employing RTCVD processes in the fabrication of future generations of highly-integrated ICs.
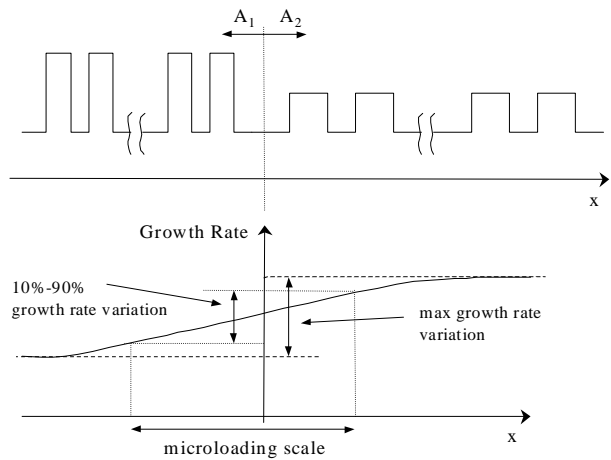

Figure 1. Growth rate variation in the vicinity of two adjacent microstructures.
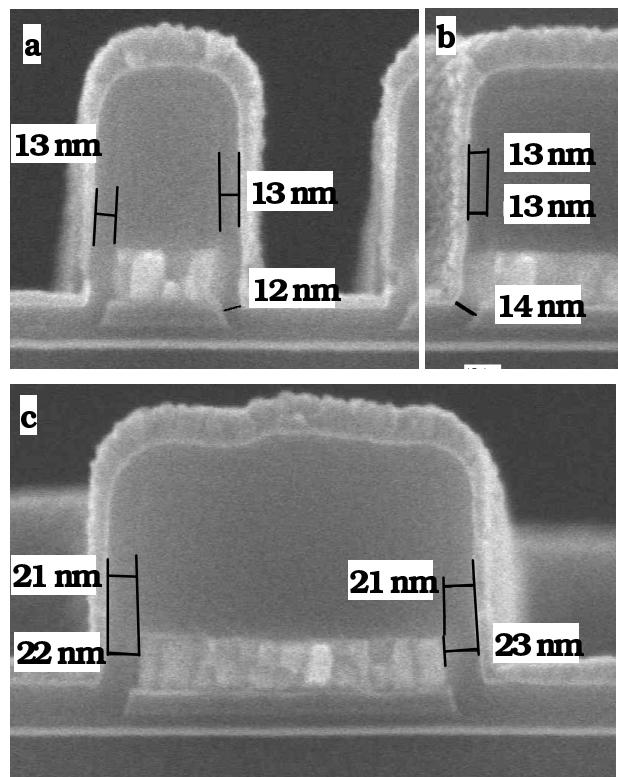

Figure 2. SiN gate spacer in various parts of the chip: (a) in a dense and large memory array, (b) in a logic area adjacent to the array shown in (a), (c) in a logic area adjacent to a small memory array.
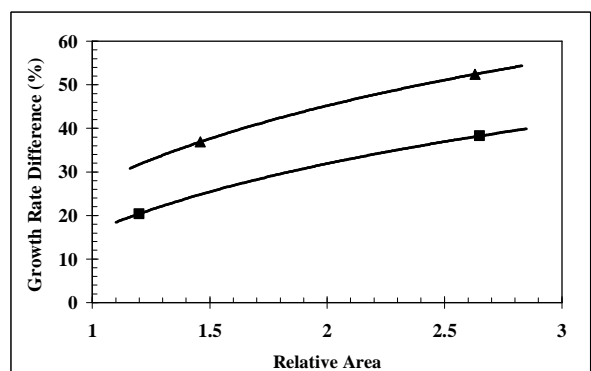

Figure 3. Growth rate variation as a function of local surface area. Triangles and squares are 110 nm and 140 nm technologies, respectively.