Molecular Beam Deposition of Alternate Gate Dielectrics for Si CMOS.

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Continued scaling of the conventional CMOS transistor will require replacing the existing SiO2 based gate dielectric with an insulating film with a higher dielectric constant in order to reach equivalent thicknesses that are 1 nm or less. In addition to the array of physical and electrical properties that this dielectric must possess, it should also be incorporated into the CMOS process with minimal perturbation of the process flow. One of the unavoidable changes will be the method of synthesis for these dielectrics.

Such a change points to a move from simple thermal oxidation of the surface silicon to form SiO2, to a deposition based process for the metal oxide (or nitride) that will most likely be a replacement. The two likely methods for this are chemical vapor deposition (and its variants) and ultra high vacuum physical vapor based deposition (UHV-PVD) techniques such as molecular beam deposition or epitaxy (MBE/MBD), with each possessing its specific advantages and disadvantages. Since there is no clear front runner as a replacement candidate for SiO2 yet, there is also considerable uncertainty as to the specific deposition method that will be used.

Chemical vapor deposition has the benefits of familiarity to tooling vendors, compliance with standard Si processing, and the ability for conformal deposition. On the other hand, there are issues with precursor residues and film purity, and complications in oxide film nucleation, often requiring a thin layer of silicon oxide to be present on the Si wafer. These disadvantages are not present for a UHV-PVD technique such as molecular beam deposition, though performance in a Si processing line and issues of throughput and reliability are big unknowns since these techniques have only recently matured (past 5 years) as production tools in the III-V industry. Additionally, this technique offers much better control over the formation of the interface between the metal oxide and silicon and is more easily scalable to larger wafer sizes since it is a line of sight technology. The pros and cons of these technique will further be discussed in the talk.

We have examined a number of metal oxide films as alternate gate dielectrics using both 2 in. and 8 in. MBE systems. The films are deposited using a metal atomic beam from a standard resistively heated effusion source and atomic or molecular beams of oxygen (or nitrogen). The atomic beams were generated using remote MBE compatible radio frequency sources. Long channel nFETs have been processed using Al2O3, AlN, and Y2O3 dielectrics and aluminium metal electrodes. Measured peak electron mobilities are in the 100-270 cm2/V-s range with Al2O3 being the most promising, though electron mobilities are still inferior to that obtained with a standard SiO2 dielectric. Physical and charge trapping characteristics of these dielectrics will be discussed.

The various films being explored for gate dielectric applications may be classified into two categories: epitaxial and non-epitaxial (polycrystalline or amorphous films). Typically, non-epitaxial films have been explored by both CVD and molecular beam approaches, and the FET data shown has been for films that are polycrystalline (Y2O3, AlN) and amorphous (Al2O3). Epitaxial films have exclusively been grown by MBE till now and if the replacement dielectric is an epitaxial one, MBE would bethe technique of choice. We have recently demonstrated an epitaxial lanthanum yttrium mixed oxide that can be lattice matched to silicon and grown by MBE. These films crystallize in the cubic bixbyite structure with a lattice constant that is approximately twice that of silicon. By adjusting the La:Y composition ratio, the lattice constant can be made to be exactly twice that of silicon. When grown on Si(111), transmission electron microscopy studies indicate uniform two dimensional epitaxial films of high quality with low extended defect densities and x-ray diffraction studies . Molecular beam epitaxy of oxides on silicon substrates represent specific challenges that can be both process related (such as the presence of oxygen in the chamber) and materials compatibility related, such as valence and bonding mismatch at the semiconductor-oxide interface. These will be discussed in the talk.