Atomic Layer Deposition Technology for Advanced Gate Stack Engineering

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In recent years the introduction of new materials and technologies into the semiconductor manufacturing is becoming a more frequent choice as the industry continues advancing on the path of improving device performance while lowering costs. One of the great challenges facing us today is the scaling of the gate stack (1). The quest to replace the SiO_2 with a higher dielectric constant material has encompassed the oxides of about half of the elements in the periodic table and is still unresolved. Similarly, a variety of deposition technologies are being evaluated for FEOL applications. In particular, a lot of interest has been generated by atomic layer deposition (ALD), due to the many benefits inherently offered by this technology (2).

At Genus, ALD was developed on a commercially established *LYNX 2* platform. A variety of high K oxides and metal nitride materials have been demonstrated using *LYNX 2* ALD tools (3-6). Flexibility built into the hardware and software allows the engineering of interfaces and complex alloy and nanolaminate structures with high precision, reliability, and competitive throughput.

This presentation will review our current results on high K oxide materials. We will focus on the deposition and characterization of HfO_2, Al_2O_3, and Hf-Al-O composite alloys and nanolaminate structures, which are among the promising gate oxide materials.

Maturity of a new technology, such as ALD, has many criteria to satisfy. Key metrics include definition of a wide and robust process window and marathon performance with tight margins on uniformity, composition, particles, conformality, contamination levels, etc., which need to be all simultaneously met (5, 6). Additionally, throughput is optimized for each specific application through a careful balance of performance requirements, such as uniformity or conformality specifications and tool maintenance schedules. We will use the deposition of HfO_2, Al_2O_3, and Hf-Al-O composite alloys to highlight the stepping stones on the commercialization pathway for ALD.

As the interface between the Si and the high-k dielectric is of foremost importance for device performance, methods for surface treatment prior to the oxide deposition will be addressed. Metal nitride ALD will be briefly covered for its potential application in metal gate engineering. Additionally, key learning from ALD process transfer from 200 to 300 mm wafer size will be discussed.

References:

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