Pattern Effects in RTP: Still a Hidden World in Production?

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Background:
The driving force for pattern related thermal nonuniformities in RTP is the color temperature difference between the heating source(s) and the patterned substrate material. Other major factors include the emissivity variation of the patterned wafer surface, the density, wavelength range and incident angle of the heating light, geometry and arrangement of the heating elements and reflectors and effective chamber reflectivity. Depending on ramp rate, the transient nonuniformities may be several times larger, than the steady state non-uniformities because of the high power density of the light flux during heating up. As long as the length scales of the optical differences in the wafer were smaller than the thermal diffusion length of Si at the process temperature, pattern effects were a "hidden world" of process evaluation in device production. The nearly simultaneous advent of large and complex chips including reduced feature sizes in the sensitive sub-0.18 μm range, and the need for fast ramp processing may make pattern effects a major concern.

Results and Discussion:
In this article we will discuss some different aspects of the pattern related process nonuniformities in lamp based RTP systems. We will show that these nonuniformities can be dramatically reduced in dual side-heated Mattson RTP systems.

1. We prepared dual side polished 200 nm SiO_2 + 110 nm poly Si coated chess board patterned wafers with 1 x 1 cm^2 squares. RTO was performed at 1150°C for 30s in dual side heated system and in another system that only heats from the front. As a third comparison a special blackbody cavity arrangement was used in the dual side heated equipment. We evaluated the oxide thickness variation along the chess board patterns, measured on the polished backside of the wafers. The calculated local temperature variation was ΔT= 45°K in case of front side heated system. The dual side heating resulted in ΔT = 25 K variation, while the creation of a blackbody cavity at the frontside of the wafer reduced the temperature variation below ΔT = 5K [1].

2. Local arising large thermal gradients may cause pattern shift and in worse case slip lines in IC production. Large pattern shift degrades yield, smaller pattern shift may broaden parameter distribution and degrade reliability of the devices. Variation in heating technology was used in BICMOS production in different split lots as a comparison to the standard dual side heating. The process was BPSG reflow at 1063°C for 7s. The ramp up rate was 50 K/s. The new heating method reduced pattern shift in case of different device designs. The improvement was a factor between 2.5 and up to 5. Simultaneously the distribution of the electrical parameters was improved to a much narrower range [2].

3. Experts in IC industry have frequently realized that even if a transistor size and design is the same in a complex device, the electrical performance of each transistor may depend on the difference of the surrounding space or material variation. One reason for this can be that pattern related local temperature differences influence process results in RTP. For deeper analysis we prepared the previously mentioned dual side polished chess board patterned wafers also with integrated "Logic-arrays". The arrays were structured alternating with open windows or coated islands in 0.5 x 0.5 μm^2 up to 5 x 5 μm^2 design variation. The wafers were implanted with 1keV As in 1E15 cm^{-2} doses both in front and backsides. Soak anneals and flash anneals were performed on a total of four wafers with different heating methods. The ramp up rate for all wafers was 100 K/s. The target R_s was around 180 ohm/sq. $T_{max.}$ was optimized with similarly implanted bare metrology wafers. Boxer Cross junction depth (X_j) measurements [3] were completed on all four wafers with a total of 144 measurement points. Table 1 shows the summary of results: The blackbody cavity radically improved X_j uniformity.

Table 1:
Boxer Cross X_j measurement results in patterned wafers annealed with different heating methods:

Process	Blackbody cavity	X_j nm	Std. dev. of X_j variation
1060°C-10s	No	46,6	9.4%
1060°C-10s	Yes	48,5	5.1%
1140°C-0s	No	47,1	10.2%
1130°C-0s	Yes	44,9	2.7%

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