

Emissivity dependence of Spike Annealing in Levitor and Lamp-based heating systems

E.H.A. Granneman, C. Laviron*, A. Halimaoui**

V.I. Kuznetsov, R. Grisel, H. Terhorst,

ASM International nv, Jan van Eycklaan 10, 3723 BC

Bilthoven, The Netherlands; *LETI-CEA, Rue des

Martyrs 17, F 38054 Grenoble, France; **ST, Rue Jean

Monnet 850, 38926 Crolles Cedex, France

Formation of Ultra-Shallow Junctions requires fast heating of wafers, with ramp rates exceeding 250°C/s (1). Heating (and cool-down) must take place with good uniformity across the wafer, and, ideally, independent of any films, devices or structures present on the wafer. In short, the heating must be independent of emissivity.

In current lamp-based systems, the surface emissivity is measured, and the heating power controlled to account for variations in (global) emissivity. Unfortunately, this procedure does not work when emissivity variations are present within areas of one wafer, (e.g. die placed adjacent to non-patterned areas at the wafer edge) or within one die (e.g. large fields of capacitors and logic functions located in different parts of the device).

This was investigated by Vandenaabeele et al (2): Patterns consisting of oxidized and bare silicon squares with typical dimensions of 10-800 nm were used to create areas with different emissivity. It was found that heating up a wafer with 100°C/s to 1100°C with lamp-based RTA systems can result in temperature differences across the features up to 80°C.

In future devices, the formation of ultra-shallow junctions require much higher heat-up rates, while at the same time the allowable temperature uniformity across wafer and die must be reduced to less than a few degrees. For that reason, it makes sense to consider heating systems such as the Levitor system (3) that are not, or much less, sensitive to variations in emissivity. The Levitor system heats the wafer by floating it in gas in between two heated blocks with gaps of 0.15 mm between wafer and block. The thin gas layer ensures an very fast heating of the wafer. In nitrogen and helium, heat up rates of 300 and 900°C/s are realized (4).

In a first test on emissivity dependency of the Levitor system, wafers with different films on the back were annealed in helium. The specific film combinations were chosen such that a reasonable variation in emissivity was obtained. The resulting sheet resistance values are summarized in table 1. Note that these wafers

Type Backside film	Rs ($\Omega/\text{sq.}$)
160 nm Th.oxide, 90 nm Poly-Si	432
500 nm Th. oxide, 90 nm Poly-Si	437
300 nm Th. oxide, 130 nm Si_3N_4	441
420 nm PE-TEOS oxide	416

Table 1. Backside dependence of sheet resistance. 1 keV, $1.25 \times 10^{15} \text{ cm}^{-2}$ B implants; anneal in He. The blocks are kept at 1100 °C, and closed during 0.5 s.

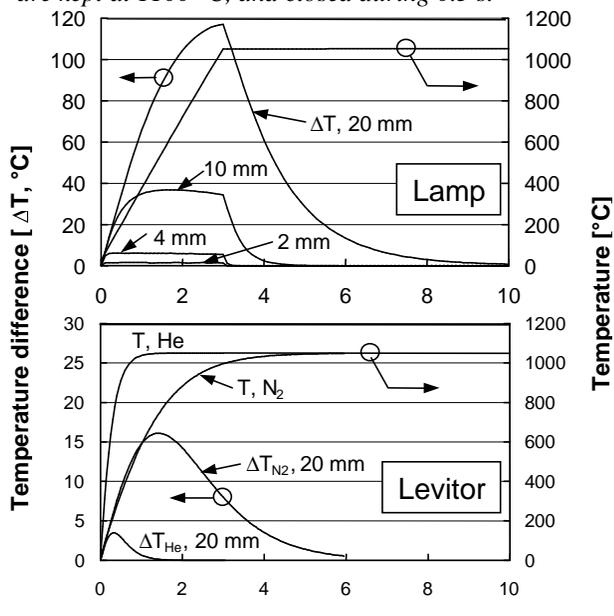


Figure 1. Temperature difference between two adjacent fields with emissivities 0.45 and 0.55, in checker board pattern with length scale 2-20 mm. In the lamp-based case a ramp rate of 350°C/s to 1050°C is assumed. In the Levitor case the gaps are 0.15 mm.

were processed in 'open loop' conditions, and the temperature of individual wafers not measured. It can be concluded that the variation of sheet resistance for different backside films is a few percent at most.

To facilitate a comparison between lamp-based systems and the Levitor for spike anneals, a 2D numerical model was made that takes into account the most relevant parameters: local variations in emissivity ϵ , feature scale length L , wafer heat-up rate dT/dt , and lateral diffusion of heat in the wafer. The 'device' was simulated through a checker board pattern with sides L . In first order, the (initial) maximum temperature difference between two adjacent fields is given by: $\Delta T_{\text{max}} \sim (\Delta\epsilon/\epsilon_{\text{ave}})(dT/dt)L^2t$.

This means that the scale length L of the fields has a very large impact. This is also illustrated by the results of the model shown in figure 1.

A comparison of both figures clearly shows that conduction heating through thin gas layers results in a much reduced temperature variation across the features.

Further details on the model, and the experimental verification will be presented at the meeting.

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