Advanced Annealing for Sub-130nm Junction Formation

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The formation of ultra-shallow source-drain extensions with low resistivity remains one of the most critical challenges on the ITRS roadmap. Progress has been made using conventional RTP process with faster heating and cooling rates for so-called "spike anneals" that have produced P-type junctions barely meeting the requirements of the 90 nm node of the roadmap, but it appears that further gains will be incremental due to the limits of the response time of both the radiation sources and the wafer itself. Other techniques such as laser thermal processing (LTP) and deposited or grown junctions have shown promise, but have severe integration problems that have yet to be solved. This paper will discuss a new lamp annealing technique called Flash-assist RTP (fRTP™) that operates in the large time gap between LTP and conventional RTP. It has shown promising results with both P- and N-type junctions easily meeting the 60 nm technology node requirements as defined by ITRS2000.

fRTP overcomes one of the fundamental limitations of lamp-heated rapid thermal processing: it is very difficult to heat, and especially, cool the bulk of a wafer. In fRTP, the bulk of the wafer is heated to an intermediate temperature using fairly conventional RTP, but then the device side of the wafer is exposed to a short (order of 1 – 10 ms) pulse or flash of intense light. The flash raises a thin layer of the wafer to a higher temperature. Since the flash duration is short compared to the thermal time constant of the wafer, the bulk of the wafer is not significantly heated. Once the flash energy is removed, the bulk of the wafer acts as a heat sink to very quickly cool the heated layer. If the intermediate temperature and temperature "jump" of the front side are chosen correctly, very high electrical activation occurs with very little dopant diffusion or change in junction depth from the as implanted position. The independent control of the flash conditions and intermediate temperature gives flexibility in junction engineering.

Figure 1 shows the simulated front side temperature during a typical fRTP process. Note that the front surface reaches a very high temperature (approaching the melting point of silicon) while the bulk temperature increases only a few degrees. Figure 2 is a series of SIMS profiles of fRTP annealed BF_2^+ implants. It can be seen that, with the choice of the correct annealing conditions, the junction depth at a concentration of 1E18cm^{-2} has barely moved during the anneal. The sheet resistance of this sample is 456 ohms per square. Figure 3 shows data of several different implant conditions annealed with fRTP positioned on the ITRS requirements. Additional data points from the literature are also shown for comparison. It is apparent that fRTP produces shallower, higher conductivity implanted layers.

Since the entire wafer surface is exposed to the flash, no scanning is required. The flash has a wide spectral distribution that couples well into silicon so no adsorbing layers or other additional process steps are needed as is the case with LTP. Further modeling and optimization are ongoing to determine the extent of this technology's utility for USJ formation. So far, process windows seem relatively wide and there is ample room for adjustment of the process. From the SIMS curves, it appears that the abruptness of the junctions is greater than in RTP, although no data on lateral abruptness has been collected.

This paper will describe fRTP annealing on various implanted samples. Boron, BF_2, and arsenic implants will be examined. The effect of pre-amorphization on the boron will also be reported. Both beamline and plasma doped implantation were used.

fRTP is a straightforward extension of lamp-based RTP technology that allows ion implant/annealing junction formation techniques to be stretched into the 40 nm technology node.

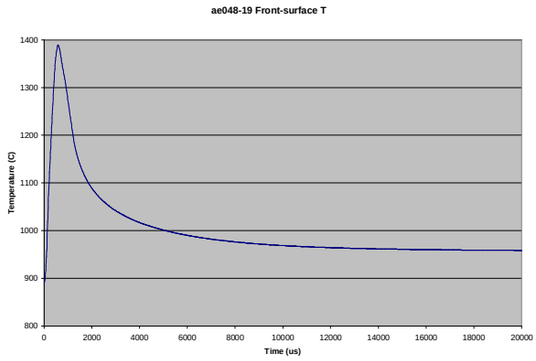

Fig. 1. Simulated front side temperature profiles during a typical flash RTP anneal cycle.

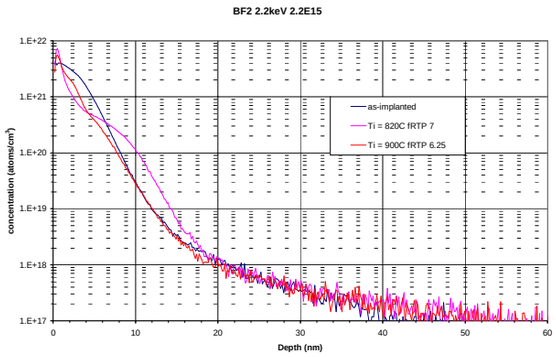

Fig. 2.SIMS curves of as-implanted and flash annealed BF_2 samples.

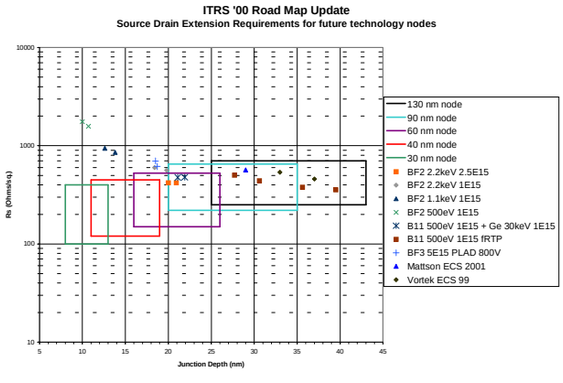

Fig. 3. ITRS2000 X_j R_s requirements showing fRTP data.