Solutions for Ultra Shallow Junctions – Improvements in spike anneal Balasubramanian Ramachandran, Ryan Boas, Sundar Ramamurthy. Transistor Capacitor Group, Applied Materials. 2727 Augustine Drive, M/S 0766, Santa Clara CA-95054

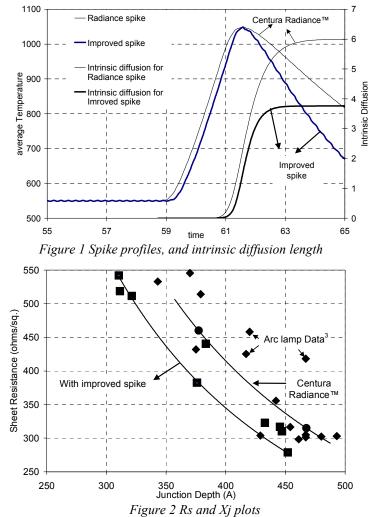
Aggressive downscaling for device dimensions to 0.10 μ m and beyond poses new and unique challenges in wafer processing¹. One of the key challenges is in field of Ultra Shallow Junction (USJ) implant anneals. Sheet resistance (Rs) and junction depth requirements, for 0.10 μ m technology and beyond, have been outlined by Sematech². Traditional Rapid Thermal Processing (RTP) systems have been unable to meet these requirements. In this paper, the USJ spike anneal technology is advanced by focusing on cool down rate. Data obtained by improving spike anneal is illustrated in this paper.

The process/hardware improvements were based on the standard Centura RadianceTM hardware. Centura RadianceTM is a production proven process tool of record for the 0.13µm node in various wafer fabrication facilities across the world. Typical temperature – time performance in the Centura RadianceTM chamber is shown in Fig 1. Improved spike demonstrates the effect of improved hardware configurations on temperature – time plots. To quantify the improvement in spike sharpness, intrinsic diffusion model was used. A >35% improvement was achieved in intrinsic diffusion length (nm) (fig. 1).

Various boron ion implants were performed using the Applied Materials Quantum Leap implanter. Wafers were pre-amorphised (PAI) with Germanium, prior to Boron implantation. To characterize the improvements a wide range of implant conditions was used. The implant energy ranged from 200eV to 500eV, and the implanted dose ranged from 1E15 atoms/cc to 2E15 atoms/cc. These wafers were then annealed with varying peak temperatures, using the "Improved spike profile". The annealed wafers were then measured for sheet resistance and analyzed for junction depth by characterizing boron profiles in silicon through dynamic Secondary Ion Mass Spectroscopy (SIMS) analysis.

The junction depth, Xj (depth in Angstrom at a Boron concentration of 1E18atms/cc as measured from the SIMS profiles) vs. sheet resistance (Rs) plot is shown in Fig.2 (squares). Also included in this plot are Rs/Xj data using the standard Centura Radiance[™] chamber (circles) and performance on an Arc lamp based system³, (rhombus). An improvement of >10% is attained, by using the Improved spike profile, over the standard Centura Radiance[™]. Also, this spike anneal process compares favorably with the available data on spike anneal processes on other RTP systems.

Detailed TED modeling^{4 & 5} was performed for various spike profiles on 500eV, 1E15atoms/cc Boron implants with PAI. Also TED effects with the same PAI wafers were also studied as part of the experiment. Details of the TED effects & modeling will be presented at the conference.



Acknowledgements:

We acknowledge the support & efforts of Raman Achutharaman, Amir Al-Bayati, Wen Chang, Houda Graoui, Abhilash Mayur, Gia Pham, and Toni Wisco from the Transistor & capacitor Group at Applied Materials. **Reference:**

- H.R. Huff, G. A. Brown and L. A. Larson, in RAPID THERMAL AND OTHER SHORT-TIME PROCESSING TECHNOLOGIES II/2001, D. L. Kwong, K. Reid, M. C. Ozturk, P. J. Timans, F. Roozeboom, Editors, **PV 2001-9**, p. 586, The Electrochemical Society Proceedings Series, Pennington, NJ (2001).
- 2. International Technology Roadmap for Semiconductors (ITRS), 1999 Edition, SIA.
- Tichy R., Elliott, K., McCoy, S., and Sing, D., 9th International Conference on Advanced Thermal Processing of Semiconductors- RTP, 2001.
- Amitabh Jain in RAPID THERMAL AND OTHER SHORT-TIME PROCESSING TECHNOLOGIES I/2000, Fred Roozeboom, Mehmet C.Öztürk, Jeffrey C. Gelpey, Kimberly G. Reid, Dim-Lee Kwong, Editors, PV 2000-9, p.524, The Electrochemical Society Proceedings Series, Pennington, NJ (2000)
- 5. C.S.Rafferty, G.H.Gilmer, M.Jaraiz, Applied Physics letters **68**, 2395 (1996)