Challenges in Transistor Scaling

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Transistor scaling has continued unabated for more than 30 years. This scaling has resulted in a dramatic decrease in all device dimensions while requiring a concomitant increase in doping concentrations. Although the advent of rapid thermal annealing and low energy implants has enabled the scaling in recent years, fundamental trade-offs are posing serious issues. This paper will discuss some of these issues as well as potential directions for continuing the historic performance trends.

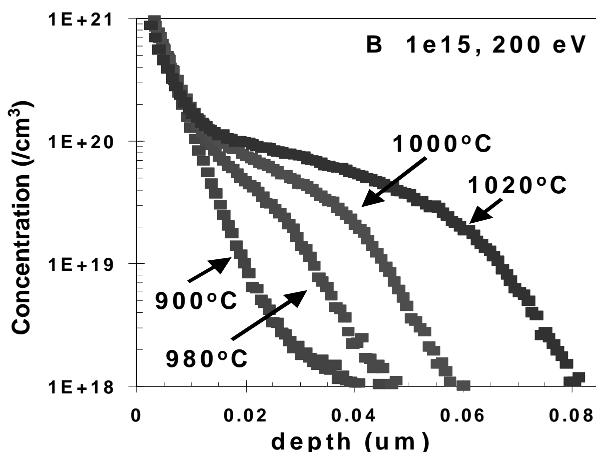
Figure 1 shows voltage potential contours for deep and shallow SDE junction depths. As can be seen, the deep SDE results in a decreased potential barrier between the source and drain, leading to larger off state leakage currents and can ultimately result in uncontrolled device characteristics.

Diffusion in silicon occurs through dopant-defect interactions that are strongly affected by ion implantation. Due to point defect annealing kinetics, short, high temperature anneals can be used to minimize these transient enhanced diffusion (TED) effects. Figure 2 shows the combination of high temperature, short time anneals and low energy implants can result in very shallow junctions. Unfortunately, although these shallow profiles due permit gate length scaling, they exhibit unacceptably high resistance (Fig. 3). In order to reduce this parasitic resistance, higher substitutional dopant concentrations are needed. However, above a certain concentration the dopant atoms are no longer substitutional, forming extended defects instead.

The strong interaction of dopant atoms, defects and annealing kinetics determines maximum active dopant concentrations. Ideally, extremely short, very high temperature anneals are optimum for producing shallow, low resistance doping profiles using ion implantation. However, taken to an extreme, other problems can arise. Laser annealing is such an extreme the benefits and issues will be discussed.

This talk will focus on the requirements and issues for scaling transistor dimensions into the ultra deep submicron regime. The pros and cons of several of the most promising directions will be discussed.

Fig. 1 – Voltage potential contours showing the effect of junction scaling on source/drain barrier.



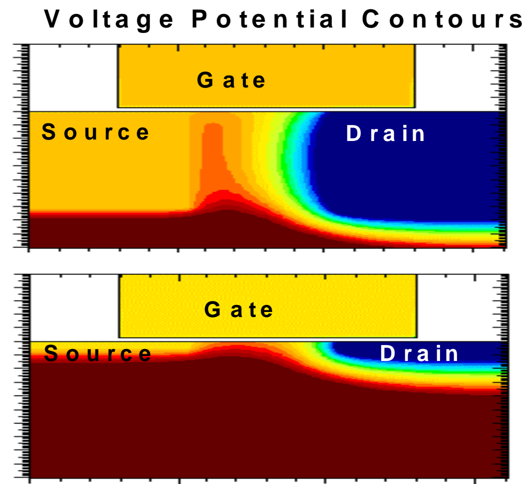


Fig. 2 – Junction depth for a 1e15, 200 eV boron profile annealed from 900 – 1020 °C for 10 sec.

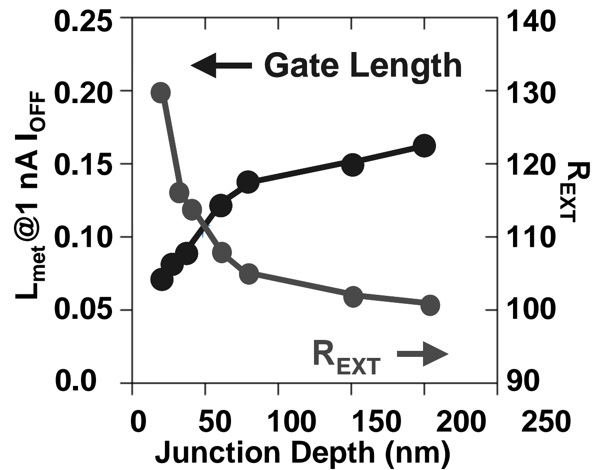


Fig.3 – Gate length scaling (Lmet) and device resistance (Rext) as a function of junction depth.