Ultra Shallow Junctions for Sub 0.1 Micron Technologies and Beyond

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This paper is an overview of the latest approaches to achieve equilibrium and above equilibrium electrical activation of the source/drain extensions for the 70 nm CMOS technology node and beyond. Topics include low energy ion implantation/spike rapid thermal anneal with provision for interstitial gettering, solid phase epitaxy, laser thermal annealing for dopant activation, and selective chemical vapor deposition of heavily doped silicon germanium following selective silicon recess. For each technology this paper reviews the projected targets, process and integration challenges, and the viability of the approach for drain extension junction depths and sheet resistance targets imposed by National Technology Roadmap for Semiconductors. Conclusions will be supported by empirical observations and materials and electrical characterization results, as appropriate. The primary focus of this paper is on p-MOS, which has traditionally posed more challenges in achieving the optimum junction depth required to maximize the transistor drive current for a given metallurgical channel length and off-state current. This technology review will also include the significant tradeoffs between short channel effects attributed to deep junctions and the parasitic resistance of shallow junctions. Moreover, this paper will present the process implications of cobalt and nickel salicide contacts on super abrupt shallow junctions.