INTEGRATION OF SOURCE-DRAIN CONTACTS INTO EMERGING FUTURE GENERATION CMOS DEVICES,

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As CMOS technology scales to gate lengths of 50 nm and below, several alternative technologies afford potential improvements to bulk Si devices, including double gate, strained Si/SiGe CMOS and silicon-on-insulator (SOI). This talk highlights the challenges to making low resistance device contacts in these alternative technologies, with emphasis on both process and silicide materials issues.

In SOI devices, the body thickness of the silicon layer will decrease below 50 nm, which requires more stringent control of the P/N junction formation and junction contact processes. Process schemes to minimize silicide contact resistance and junction de-activation in scaled SOI devices including silicide with RSD and laser silicidation are reviewed, with highlighting of outstanding challenges still associated with such techniques.

Also discussed are problems associated with contacting vertical double gate devices, where additional process integration constraints are imposed due to the necessity of forming a symmetrical contact to a free-standing Si source/drain.

Finally, the case of strained Si/SiGe CMOS presents an additional set of materials challenges because silicidation of SiGe S/D is more complex than in the pure Si system. Issues including silicide phase formation, thermal budget and dopant interaction in SiGe-based silicidation are detailed.