Polysilicon CMOS TFTs inverters with a gate silicon oxide deposited using PECVD with hexamethyldisiloxane (HMDSO)

G. Gautier¹, N. Coulon¹, C.E. Viana², S. Crand³, R. Rogel¹, N.I. Morimoto and O. Bonnau².

¹GMV, Université de Rennes 1, bat. 11B, 35042 Rennes CEDEX, France.
²LSI, PEE, EPUSP, Av. Professor Luciano Gualberto, 158, Trav. 3, 05508-900 Sao Paulo, SP, Brazil.

The demand for high resolution AMLCDs (Active Matrix Liquid Crystal Displays) resulted in a considerable increase in efforts to develop poly-Si TFT’s (Thin Films Transistors). High-resolution (> one million pixels) and large-size TFT-LCD’s have been developed as well as new driving methods and pixel structures have been proposed. Using polycrystalline silicon TFTs, the peripheral drive circuits can be integrated on the same substrate, reducing the number of external drivers and connections. These reductions would lead to a large improvement in reliability and potential cost decrease [1].

In previous work, we have developed a fabrication process of polysilicon CMOS TFTs using SPC and LPCVD techniques [2]. This process involved a gate silicon oxide deposited at 450°C by APCVD and annealed during one hour at 600°C.

In this paper, we propose a transistor structure where the doped and undoped silicon layers are deposited during the same growth process introducing the doping gas (phosphine or diborane) in the reactor [3]. This technique, combined with the use of a 40 nm thick PECVDb-HMDSO (Hexamethyldisiloxane with O₂ active feed gas) silicon oxide as the gate [4], produces high performances N and P type TFTs, as shown in Table 1.

Table 1 :N and P type average electrical parameters of CMOS-TFTs.

<table>
<thead>
<tr>
<th></th>
<th>V_T (V)</th>
<th>μ_FE (cm²/V.s)</th>
<th>S (V/déc)</th>
<th>I_ON/I_OFF</th>
</tr>
</thead>
<tbody>
<tr>
<td>N Type</td>
<td>1.6</td>
<td>97</td>
<td>0.68</td>
<td>2x10⁶</td>
</tr>
<tr>
<td>P Type</td>
<td>-5.9</td>
<td>53</td>
<td>0.87</td>
<td>3x10⁶</td>
</tr>
</tbody>
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The transfer characteristics of typical TFTs are shown in Figure 1 for a width/length ratio of 1/3 and 5/3 for N and P type respectively.

Figure 1: Transfer characteristics of N and P type TFTs in the linear region.

These characteristics present very well agreement with previous work using an APCVD silicon oxide gate.

CMOS-TFTs inverters were also characterized. The transfer characteristics present very abrupt transition when V_DD > V_{TN} - V_{TP} (Figure 2) with a maximum average gain of 190 for V_DD = 10 V. The transition voltages (V_{IT}) as well as the noise margins (NM_H and NM_L) are far from the ideal value of V_{DD}/2 but can be improved increasing β (eqn1 to (W/L)β/(W/L)α).

Indeed, for V_DD = 10V, V_{IT} can reach the value of 3.9 V for β = 5 (instead of 2.95 V for β = 1).

Figure 2 :Transfer characteristics of typical CMOS-TFT inverters for various power supply voltages (V_{DD} = 5, 7.5 and 10 V).

Some ring oscillators were also characterized (Figure 3). They present a maximum oscillation frequency of 34 kHz for V_DD = 15 V which corresponds to an average propagation delay of 3.3 μs.

Figure 3 :Operation frequency of a 9-stage CMOS-TFT ring oscillator as a function of V_DD.

REFERENCES