Controlled Filling of Silicon Trenches with Doped Oxide for MEMS

Ajay Agarwal and Ranganathan Nagarajan
Institute of Microelectronics, 11 Science Park Road,
Singapore Science Park II, Singapore 117685
Phone: (65) 6870 0125 Fax: (65) 6777 0670
Email: agarwal@ime.a-star.edu.sg

Abstract

In the fabrication of MEMS, anisotropically etched trenches are often used. These trenches are made using deep reactive ion etching and then refilled with either silicon oxide or the combination of silicon oxide and polysilicon using LPCVD process. The oxide in trenches serves either as isolation layer between electrically active areas or as sacrificial layer. This paper presents a new method of refilling the trenches by doped silicon oxide in the controlled fashion and its advantages. Using this method, a hole can be trapped inside the trench whose length can be varied from 80 to <10 percent of that of trench depth, by depositing doped oxide at low pressure in SACVD reactor, followed by furnace heat treatment.

Normally, silicon oxide is filled in trenches by using LPCVD at few hundreds of millitorr pressure. Figure 1a shows such a filling while figure 1b is a result of silicon oxide filled by SACVD at 200T. The trench filling by normal SACVD process is highly non-conformal and hole trapped inside the trench opens-up as the surface oxide is etched in the subsequent planarization process. The trenches filled by low-pressure (50T) SACVD, followed by removal of surface oxide are depicted in figure 1c. The holes trapped here are well covered even after the removal of surface oxide. The keyholes formed by such process can be further squeezed (if required) by heat treatments as shown in figures 2 a – c.

A typical application is shown in figure 3 where trenches, filled with sacrificial oxide, are made to surround the silicon structures that are released by etching the oxide in hydro fluoric acid solution after KOH ECE etch stop, from the back side of the wafer. Due to partially filled trenches, the release time of the silicon blocks can be drastically reduced. The advantage in the usage of such oxide contours also lies in the selection of alternative silicon oxide etchant, ECE metal, protection layer, and their easy removal techniques. Such oxides can be easily etched out using much diluted hydro fluoric acid solution, which further complements the usage of photo resist in place of silicon nitride, as protection layer of the devices and structures on the front side of the wafer (fig 3).

Overall, this technique provides a cost-effective solution compared to other release process sequence that uses trenches filled with LPCVD silicon oxide. Various components for optical MEMS such as electrodes, cantilevers, mirrors, etc. have already been fabricated successfully using this partially filled trench methodology. The detailed process steps and the results of the example structures will be presented.

References

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Figures

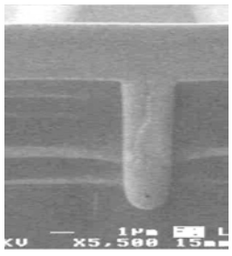

Fig 1a: Silicon oxide filled in the trench by LPCVD.

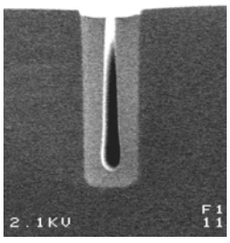

Fig 1b: Silicon oxide filled in the trench by normal SACVD and surface oxide etched.

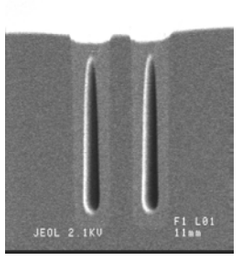

Fig 1c: Partially filled trenches using new SACVD method and surface oxide etched.

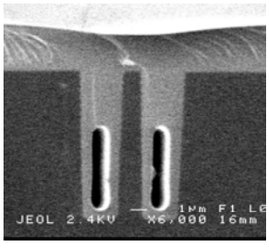

Fig 2a: Squeezed holes after heat treatment at 900°C for 2 hrs

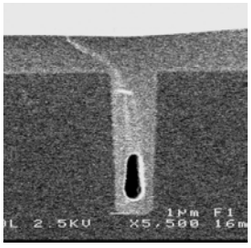

Fig 2b: Squeezed hole after heat treatment at 900°C for 6 hrs

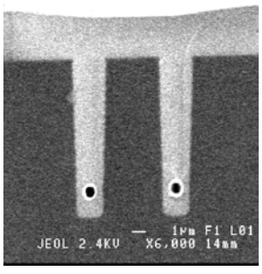

Fig 2c: Squeezed hole after heat treatment at 900°C for 10 hrs

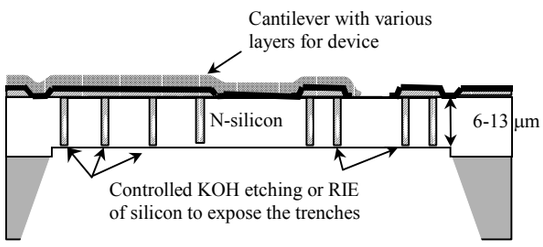

Figure 3: Wafer after controlled KOH etching or RIE of silicon to expose trenches.