Challenges for the Application of High-ε Gate Dielectrics in Future CMOS Technologies

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The aggressive scaling of CMOS devices is quickly driving SiO_2 as a gate dielectric to its limits [1]. Therefore, it is planned to use insulators with high dielectric constant, ε, within 2-5 years. [2] It is the intent of this change to keep the gate leakage current and its contribution to the power consumption in CMOS technologies at an acceptably low level. If high-ε dielectrics cannot be developed in time, device scaling may not be possible at the projected rate
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The high-ε dielectric of choice will likely be a deposited film produced by either a chemical vapour deposition technique (ALD, MOCVD, and others) or one of the many other methods under investigation (such as PVD [3,4], JVD, MBE). Especially for the CVD based methods, deposition temperatures are rather low (300 – 600 ^oC), resulting in highly defective films on an atomic scale. It is the objective of the ongoing, worldwide high-ε efforts to demonstrate that the excellent *electrical* properties of thermally grown SiO_2 – which serves as a benchmark for any future gate dielectric - can be met with deposited high-ε films.

Some of the most studied high-k candidates include Al_2O_3 [4,5], ZrO_2 [6], HfO_2 [13] Y_2O_3 [4], or La_2O_3 [4], as well as mixed oxides containing SiO_2 (silicates) [7-9] or Al_2O_3 (aluminates) [10] and metals like Hf [8], Zr [8], Y or La [9]. Others use multi layers including two or more of these oxides [11]. With many of these materials, electronic devices (capacitors and field effect transistors (FET)) have been built, indicating that some of the CMOS integration challenges can be met. [12] However, with respect to their *electrical* performance and stability, many results in the literature show that much work is needed to match or exceed the electrical performance, stability and reliability of state-of-the-art CMOS devices with SiO_2. [13-21]

In this invited contribution, some of the electrical properties of high-ε gate stacks will be reviewed, focusing on ALD deposited Al_2O_3 and HfO_2 containing stacks. Issues of charge trapping, mobility degradation and reliability will be addressed. An attempt will be made to connect these problems by discussing the impact of charge trapping on mobility [13-16,23] and reliability [24,25]. By studying charge trapping in thick films, it can be demonstrated that the high-ε layers are highly defective and exhibit a complex charge trapping behaviour. It can be shown that the observed charge trapping in thick layers persists also in scaled layers required for future applications. Fast measurement techniques have to be used to fully evaluate the charge trapping in scaled stacks. The discussed results indicate that optimisation of the bulk properties may be needed for successful integration of many high-ε dielectrics.

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