POTENTIAL FLUCTUATIONS IN HIGH-K BASED DIELECTRIC MOS DEVICES

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It is well-known that capacitance-voltage (C-V) characteristics of non-ideal MOS structures can be stretched out along the voltage axis. This voltage stretch-out is generally attributed to an increase in the interface trap level density whereas a pure shift of the C-V curve towards negative (resp. positive) voltages is due to the presence of positive (resp. negative) charge in the oxide [1]. Other sources have been also identified for this stretch-out effect, for example the random nature of the dopant distribution at high doping levels or local oxide thickness fluctuations in ultra-thin oxide devices [2].

In this study, we show that a lateral non-uniform oxide charge distribution in MOS devices can also induce a stretch-out of the capacitance-voltage characteristics. The origin of this effect is due to fluctuations in the surface potential which varies laterally over the area of the device. These effects are thoroughly analyzed using a full homemade numerical code (CAPA2D), based on the two-dimensional solving of the Poisson equation in the structure using a finite difference scheme on a uniform mesh (Fig. 1). For example, the presence of a ponctual charge repartition located in the interior of the oxide just above the oxide/semiconductor interface induces important 2D potential fluctuations in the underlying semiconductor region (Fig. 2a) and especially at the semiconductor surface (Fig. 2b). The direct consequence is a visible stretching of the C-V characteristic, illustrated in Fig. 3, as compared to the reference curve for which the gate stack is totally free of charge. This very simple example immediately shows that this stretching effect is different from the one obtained when considering interface traps. Further, the influence of several oxide charge patterns on C-V characteristics is systematically investigated: (a) linear or gaussian distribution in the interfacial oxide, (b) random distribution in the stack (Fig. 4), (c) charged grain boundaries in the high-k layer. We also demonstrate that full 2-D simulation is mandatory to take into account these effects, since a simple 1-D approach does not capture the influence of non-uniform charge distributions (Fig. 3).

This work has been performed in the particular case of high-k material based devices. Indeed, it has been experimentally shown that such gate dielectric stacks can present a rather good interface quality with the underlying substrate (due to the presence of a SiO_x thin interfacial layer) but, in the same time, exhibit highly stretched C-V curves [3]. Because interface states cannot be invoked in this case, the non-homogenous nature of such deposited gate stacks (in terms of oxide charge) could be at the origin of the observed C-V behavior.

Finally, the present analysis will be extended to MOSFET devices, where the lateral non-uniform charge distribution is expected to induce important threshold voltage fluctuations and transconductance degradation.

References

[1] S.M. Sze, Physics of Semiconductor Devices, Wiley NY, 1981.
[2] E. Nicollian and J. Brews, MOS Physics and Technology, Wiley, NY, 1982.
[3] M. Houssa et al., Applied Physics Letters 77, 1885, 2000.

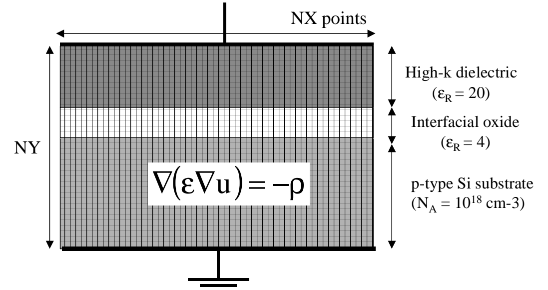

Figure 1. Schematic representation of a MOS structure with a two-layer gate dielectric stack.

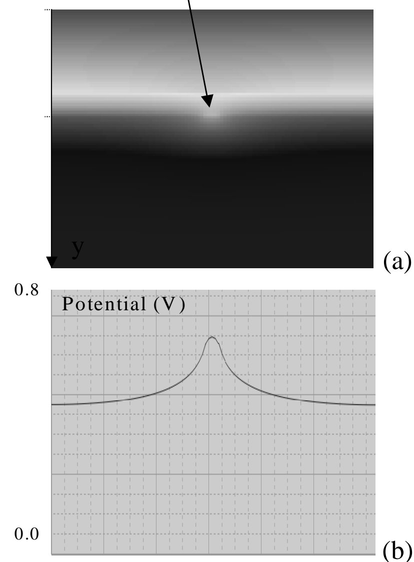

Figure 2. a) 2D potential distribution in the MOS structure resulting from the presence of a ponctual fixed oxide charge. b) Corresponding lateral variations of the surface potential at the silicon surface.

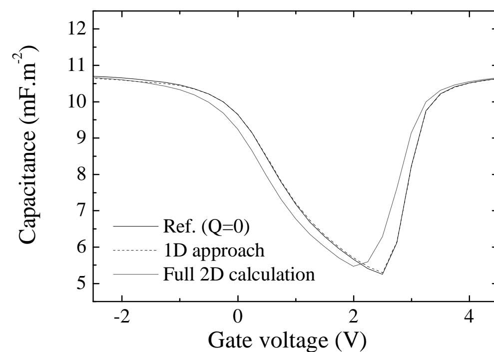

Figure 3. C-V characteristic calculated with CAPA2D considering the charge distribution defined in Fig. 2. The reference curve (no charge in the gate stack) and the one obtained with the 1-D approach is also plotted.

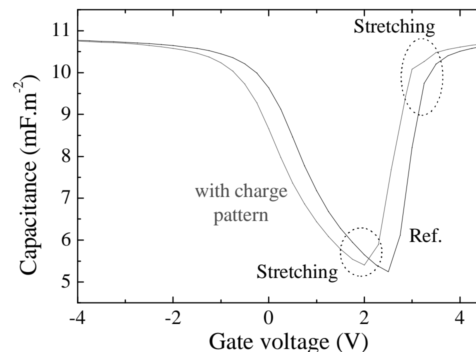

Figure 4. Impact on the C-V characteristic of a random charge distribution in the gate stack. The reference curve (no charge in the gate stack) is also plotted.