Investigation of barrier layers for Cu-ultra low k porous SiLK^{TM} integration

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Barrier layers play a crucial role in Cu-low k integration. In this work, three kinds of barriers (Ta, TaN and Ta/TaN) deposited on a ultra low k dielectric, porous SiLK^{TM} film were investigated using various techniques which include four probes, X-ray diffraction (XRD), Atomic force microscopy (AFM) and transmission electron microscopy (TEM). It is found that Ta barrier layer has lower resistance, but bigger grain size and more grain boundary defects which cause fast diffusion. Longer diffusion depth can be observed at the interface of Ta/porous SiLK after being annealed at 500^{o}C for 3 mins. TaN barrier layer shows smaller grain size and shorter grain boundary because N atoms were incorporated into Ta lattice. It is efficient in reducing diffusion but the higher resistance of the barrier layer is not desirable for a barrier layer. It is observed that compared with Ta and TaN, the multi-stacked Ta/TaN is a better choice of barrier layer as it has not only lower resistance but also good thermal stability as well as few grain boundary defects.

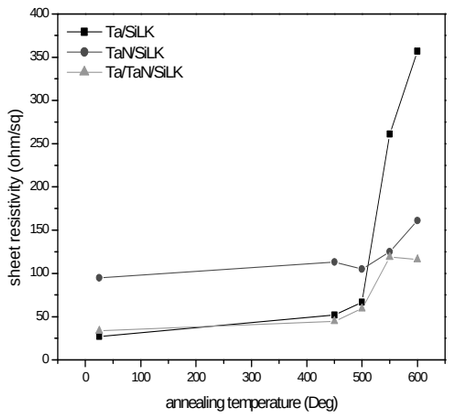
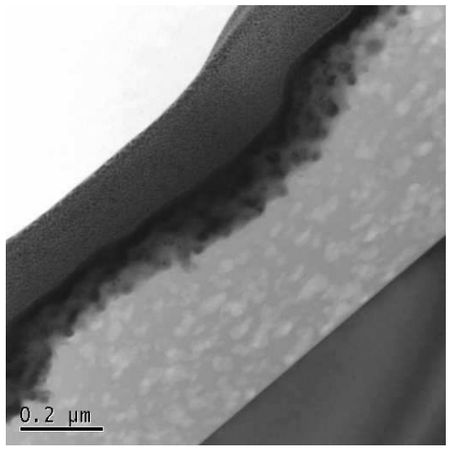
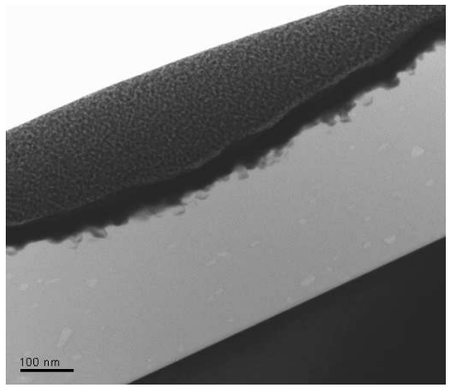


Fig. 1 sheet resistance of three barriers changing with annealing temperature



(a)



(b)

Fig.5 TEM images of (a) Ta and (b) multi-stacked Ta/TaN barriers on porous SiLK after being annealed at 550^{o}C for 3mins