$Si-SiO_2$ interface trap properties and dependence with oxide thickness and with electrical stress in MOSFETS with oxides in the 1-2 nanometer range

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With the continuing decrease of MOS device dimensions, conventional electrical characterizations such as capacitance-voltage (C(V)) measurements from which oxide thickness, doping concentration profiles or $Si-SiO_2$ interface trap densities were extracted in a simple manner, are not possible anymore. This is due primarily to the large tunneling currents flowing through the oxides as soon as small gates biases are applied to the structures. This also results from quantum mechanical effects [1, 2] .

In recent years, a lot of work has been devoted to modeling C(V) characteristics of MOS structures with oxides in the nanometer range [3] and extracting oxide thickness [4] but up to recently, interface trap densities were not extracted from such measurements.

This point is of importance as interface trap density, D_{it}, extraction has always been a standard characterization tool for MOS technologies. A possible dependence of D_{it} with oxide thickness has been addressed many times in the literature [5-7], especially in relation with the stress at the $Si-SiO_2$ interface due to lattice mismatch [8] or with SiO_2 interface roughness [7, 9]. In conventional MOS structures with thick oxides, an annealing at high temperature follows high temperature thermal oxidation, allowing relaxation of the stress in the oxide, while a low temperature annealing under hydrogen reduces the interface trap density to values in the low 10^{10} eV^{-1} cm^{-2} range. From etching experiments, a strained interfacial layer around 1 nm thick has been widely measured [10, 11].

In MOS structures with ultrathin oxides grown well below 900°C, interfacial as well as bulk oxide relaxation are extremely slow so that all the oxide film is stressed [12] and oxide thickness becomes of the order of the strained interfacial region measured on thicker oxides.

Due to the absence of reliable techniques for D_{it} measurements on such structures, models based on carrier tunneling and relying the stress induced leakage current (SILC) to the creation of $Si-SiO_2$ interface or near interface traps have been proposed [13, 14].

Recently, it has been shown that it was possible to extract reliable D_{it} values in MOS structures with oxides down to 1.2 nm. This has been achieved using the charge pumping method in the small gate pulse mode [15, 16]. By doing so, any degradation of the oxides is avoided and the tunneling currents are strongly reduced with regard to the current of interest. Interface trap capture cross sections can also be extracted from the measurements [17].

After recalling the principle of the method and discussing its reliability and accuracy with regard to charge pumping mechanisms and to quantum mechanical effects, the evolution of the $Si-SiO_2$ interface trap densities and of the trap capture cross sections for devices with oxide thickness ranging from 2.3 to 1.2 nm, will be presented. The results will be discussed with regard to the oxide thickness and to oxide and interfacial stress.

Finally, the evolution of D_{it} under electrical stress will be addressed. The results will compared with those obtained from the models relying the oxide trap density to the stress induced leakage current [13, 14].

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