Role of Ultra Thin Silicon Dioxide Interfacial Layer in High Performance High Dielectric Constant Gate Dielectrics

R. Singh [1, *], M. Fakhruddin[1], K. F. Poole [1],
S. V. Kondapi [1], J. Narayan [2] and S. Kar [3]

[1]Holcombe Dept. of Electrical and Computer Engineering and
Center for Silicon Nanoelectronics
Clemson University
Clemson, SC 29634-0915
[2]Department of Materials Science & Engineering
North Carolina State University
Raleigh, NC 27695-7916
U. S. A.
[3]Department of Electrical Engineering
Indian Institute of Technology
Kanpur-208016
India

[*] Email: srajend@clemson.edu

In order to continue manufacturing low-cost semiconductor products with improved performance, reliability and functionality, manufacturing beyond 70 nm nodes poses many new process integration challenges. [1]. One such key new challenge include introduction of new materials and new processes. Specifically, the introduction of a new gate/high-κ dielectric process is one of the most challenging issues faced by the silicon IC industry. In order to push silicon down to its fundamental limit of 6-8 nm feature size circuits, the optimized equivalent oxide thickness should be about 1 nm or less.

In a recent publication [2], we have shown that rapid thermal processing assisted atomic layer deposition of ultra thin ZrO_2 films leads to significant reduction in leakage current density as well as increase in the capacitance per unit area. The processing steps include in-situ cleaning of silicon surface, in-situ deposition and in-situ annealing. At 1V, our ZrO_2 film of 2.4 nm thickness showed a leakage current density of 1.83×10^{-11} A/cm^2 and capacitance per unit area of 8.07 μF/cm^2. Achieving low leakage current density along with high capacitance per unit area demonstrates the superior performance of our process. The density of traps measured after constant current stressing showed almost no variation as the field across the film was increased up to 9 MV/cm. The breakdown field of the 2.4 nm thick films is more than 20 MV/cm. These results show significant improvement of leakage, capacitance characteristics and reliability over other high κ results reported in the literature.

In this paper, we will present the role of the ultra thin interfacial silicon dioxide layer on the performance of high-κ dielectrics. We have performed a number of experiments to understand the role of the interfacial layer. In one experiment, we used the thermal cycle (in-situ cleaning, in-situ deposition and in-situ annealing) without using the precursor for the deposition of ZrO_2. The electrical characterizations of these films show that the breakdown voltage of the interfacial layer is about 0.15 V. The study of current-voltage (I-V) characteristics as a function of temperature suggests that the interfacial layer behaves similar to conventional dielectric layer of the silicon dioxide. A complete electrical and structural characterization of the interfacial layer will be presented.

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References

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