MODELING AND ELECTRICAL CHARACTERIZATION OF MOS STRUCTURES WITH ULTRA THIN GATE OXIDE

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The aggressive scaling of Metal-Oxide-Semiconductor (MOS) devices has resulted in the use of ultra thin oxides (3 nm and less) as gate insulator (Fig 1), in order to improve the electrostatic coupling between the gate electrode and the substrate. Indeed, the reduction of the gate insulator thickness leads to a significant increase of the current drive capability of the MOS transistor, and also to a better control of short channel effects. Moreover, huge progress in the fabrication process of Gate oxide have made possible to realize such ultra thin layers (made only of a few number of molecular layers), with an acceptable thickness roughness and uniformity, as well as with a low level of defects.

However, the use of ultra thin oxides is also responsible for the enhancement of parasitic effects, which tend to reduce the expected performance increase, and which raise new challenging issues for MOSFET designers. The increase of the electrical field at the Si/SiO_2 interface for instance (due to the use of ultra thin gate oxide and high doping level in the substrate) is responsible for strong depletion effects in the polysilicon gate and quantum confinement in the substrate, leading to a decrease of the coupling between the gate and the substrate. Moreover, the tunneling phenomenon gives rise to an exponential increase in the gate current with the thickness reduction (Fig 2). The tunnel current can significantly contribute to the MOSFET current leakage in the Off State and is by turn becoming one of the major issues in MOSFET scaling. All these effects present in MOS structures with ultra thin oxide (quantum confinement, polydepletion and tunneling) have to be carefully understood and analyzed in order to be able to design optimized CMOS devices and circuits of the next technological generations. Moreover, it should be noted that such phenomena will play an increasing role in future devices featuring high K dielectrics or sub 50 nm channel length.

In this paper, a review of the main modeling and electrical characterization issues in MOSFETs with ultra gate oxide will be proposed. In a first part, advances in the modeling of polydepletion in the gate and quantum confinement in the substrate will be analyzed and their impact on the parameter extraction from electrical measurements and numerical simulations will be discussed.

Then, the issue of modeling of direct tunneling through the gate will be also addressed.

Moreover, the impact of gate leakage on capacitance measurements will be analyzed (Fig 3) and procedure to overcome these parasitics will be discussed. Finally, the implication of gate leakage partitioning between source and drain will be addressed both experimentally and theoretically for MOSFET characterization purposes.

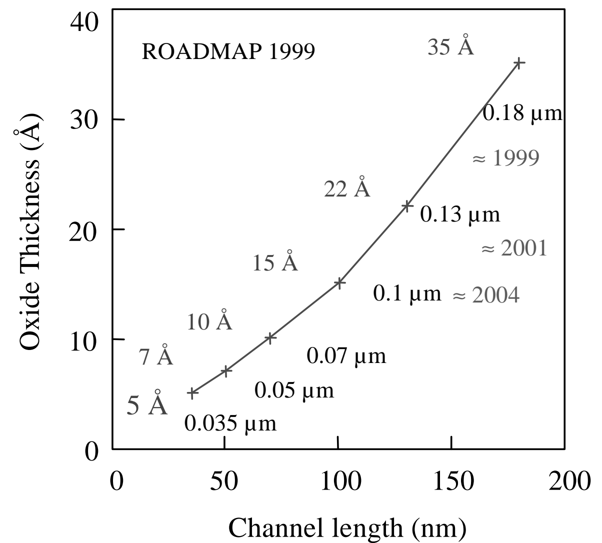

Figure 1 : Scaling of the gate oxide thickness of high performances MOS transistor according to the SIA roadmap 1999.

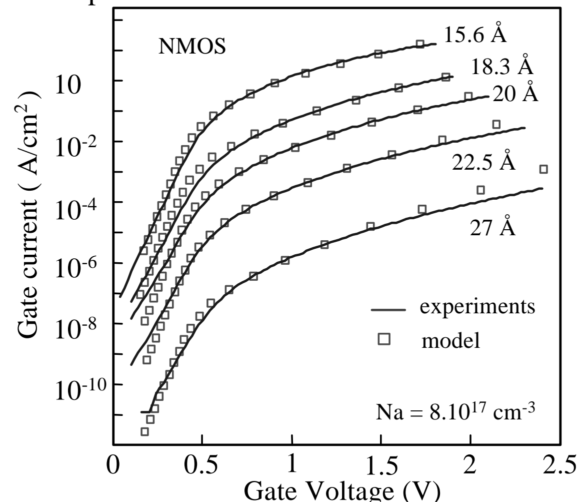

Figure 2: Gate current in NMOS transistor in inversion regime (Vd=0V). Experimental data have been fitted using the oxide thickness as only fitting parameter

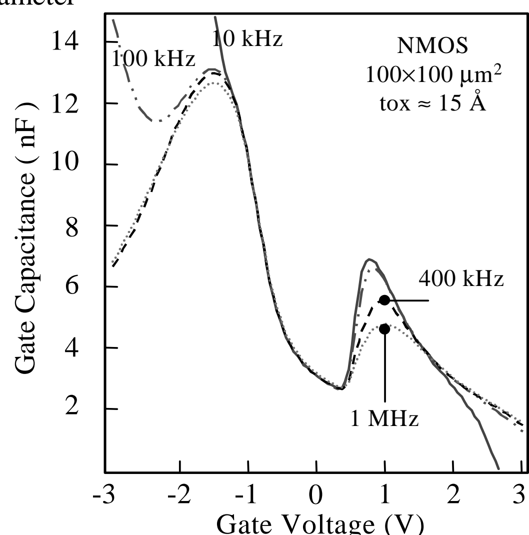

Figure 3 : Typical High Frequency C-V curves measured on large area NMOS transistors (from 10 kHz to 1 MHz).