Analysis of short-channel MOSFET behavior after gate oxide breakdown and its impact on digital circuit reliability

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Until now most of the research on gate oxide breakdown was devoted to understand the physical mechanisms that are governing the breakdown process, on the exact statistical and field or voltage acceleration models for breakdown and on the influence of processing and interface quality on the breakdown behavior [1-3]. Little work was devoted, however, to understand the electrical behavior of MOSFET's after breakdown, and how this post-breakdown behavior influences the operation of digital circuits [4-6]. Because the reliability margin for state-of-the-art devices is vanishing rapidly with the aggressive downscaling of the oxide thickness [7,8], it becomes very important to understand the impact an oxide breakdown has on the circuit behavior.

One of the major factors presently assumed to be limiting the lifetime of CMOS integrated circuits is the occurrence of the first failure (breakdown) of the gate dielectric in one of the circuit's field-effect transistors (FETs). Unfortunately, the exact extrapolation of time-to-first-breakdown at operating conditions is still difficult, since the physical mechanism governing the MOSFET gate dielectric breakdown is not yet fully understood. This was less of a problem for older CMOS technologies, where even more pessimistic reliability predictions satisfied the 10-year lifetime for 99.99% of circuits at operating conditions. However, because the probability of oxide breakdown strongly increases with decreasing oxide thickness, the present reliability criterion may qualify future downscaled CMOS technology generations as insufficiently reliable. We may therefore be entering a new realm of CMOS reliability assessment, where mild gate oxide failures are unavoidable, but because they are well understood, they can be built into the circuit design and tolerated. Consequently, the present reliability criterion may have to be redesigned.

It has been already proposed that many *soft* or even several *hard* breakdowns could occur in a circuit before it fails [4]. This opens up the possibility of relaxing the present stringent reliability criterion in some cases, e.g., high-performance logic. Such relaxation would result in a much-needed extra reliability margin. This possibility can, however, be fully explored only with thorough understanding of how exactly gate-oxide breakdown affects the FET operation.

In this paper we present a review of recent work that was carried out in this direction.

In the **first part** we analyze the impact of an oxide breakdown in a MOSFET on its electrical characteristics [5]. In order to do so, we start by describing the recently introduced methodology to determine the exact location of the breakdown along the channel of a MOSFET with nanometer resolution. Then we show that there exists a clear correlation between the post-breakdown gate resistance measured and the location of the breakdown path in the device. We show why, even though the breakdown path size remains constant, the breakdowns located over the FET channel region appear "softer" then those over the source/drain extensions, which makes them inherently less damaging for FET and therefore circuit operation.

This will bring us to propose a physical model for the post-breakdown behavior of the MOSFET. Both device simulations and circuit simulations using a new equivalent circuit model for a MOSFET after breakdown describe very well all measured currents that are flowing in the MOSFET after breakdown, including the substrate current, and this for both hard and soft breakdown. The origin of the substrate current in nFETs after gate dielectric breakdown has been in the past a subject of discussion. Several groups addressed this issue in relation with soft gate-oxide breakdown. In this paper we investigate the substrate current and show that the proposed model also naturally explains the origin of this current for all breakdown positions and for all possible stress conditions. The equivalent circuit model can be used for circuit reliability assessment.

In the **second part** we show a case study on the impact of an oxide breakdown on the functioning of a particular digital CMOS circuit for the simpler case of hard gate oxide breakdown [4]. The influence of FET gate oxide breakdown on the performance of a ring oscillator circuit is studied using statistical tools, emission microscopy, and circuit analysis. It is demonstrated that many hard breakdowns can occur in this circuit without affecting its overall function. Time-to-breakdown data measured on individual FETs are shown to scale correctly to circuit level. SPICE simulations of the ring oscillator with the affected FET represented by an equivalent circuit confirm the measured influence of the breakdown on the circuit's frequency, the stand-by and the operating currents. It is concluded that if maintaining a digital circuit's logical functionality is the sufficient reliability criterion, a non-zero probability exists that the circuit will remain functional beyond the first gate oxide breakdown. Consequently, relaxation of the present reliability criterion in certain cases might be possible. Finally, we draw on many similarities of this circuit and a general digital CMOS circuit to generalize our results.

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