New Reliability Issues of CMOS Transistors with 1.3nm Thick Gate Oxide

M. F. Li, B. J. Cho, G. Chen, and W.Y. Loh
Silicon Nano Device Laboratory, Department of Electrical and Computer Engineering,
National University of Singapore, 4 Engineering Drive 3, Singapore 117576

D. L. Kwong
Microelectronics Research Center, Department of Electrical and Computer Engineering
The University of Texas at Austin, Austin, TX 78712

Abstract: In this paper, we will discuss several new reliability issues facing CMOS transistors with ultra thin gate oxides and their impacts on projection of operation voltage V_{10Y} for 10-year lifetime. The most important findings are:

1). Oxide lifetime is more meaningfully determined by an event taking place much earlier than oxide breakdown: a strongly transistor-size dependent increment in gate leakage current. Contrary to oxide time-to-breakdown T_{BD}[1], the newly defined oxide lifetime is shorter when the transistor size is smaller.

2). By proper processing of DCIV signal[2], DCIV technique is demonstrated for direct monitoring and accurate determination of interface trap generations in CMOS devices during stresses even with t_{ox}=1.3 nm.

3).Contrary to previous reports on thicker gate oxide[3], we have shown that $V_g=V_d$ is the worst-case hot carrier degradation condition for both n-MOS and p-MOS, with p-MOS showing smaller V_{10Y} than n-MOS.

4). A "dynamic" NBTI during AC stressing is reported for the first time which clearly demonstrates that the conventional (static) NBTI[4] underestimates p-MOS device lifetime. A physical model is developed for this phenomenon. The DNBTI determines the overall CMOS device lifetime and will have significant impact on projection of maximum operating voltage in practical dynamic operation of digital circuits.

Device fabrication: CMOS devices were fabricated using standard dual-gate CMOS technology. Gate oxide of 1.3 nm thickness was grown by RTO followed by an exposure to high-density nitrogen plasma.

Interface traps measurement in CMOS devices with 1.3 nm gate oxide thickness: For n (p)-MOS, in the range of V_g=0 to -1(+1) V where the DCIV I_b peak appears, the intrinsic tunneling bulk current I_b corresponds to bulk to gate hole (electron) tunneling and is much lower than the gate current, because the holes (or electrons) face Si energy gap in the poly gate. The gate-to-interface trap tunneling current[5] is eliminated by deducting ΔI_g from ΔI_b. Further, by increasing the forward bias, the disturbance of drain-to-bulk thermal-trap-tunneling effect[6] is reduced and clear DCIV peak ΔI_{DCIV} that is proportional to the number of interface traps ΔN_{it} can be successfully obtained.

V_{10Y} projections with different stress conditions:

Oxide degradation: For 1.3 nm gate oxide, T_{BD} is too long to be considered as a limiting factor of device degradation. Instead, a steady increase in gate leakage I_g taking place much earlier than breakdown is observed. The increase of leakage current density J_g shows a strong area dependence, which implies that the oxide degradation is very much localized, unlike the uniformly distributed SILC in thick oxide[7,8]. Contrary to T_{BD} as described in [1], the oxide lifetime defined by the time it takes to reach 100% increment in I_g is shorter when the transistor area is smaller.

Hot-carrier degradations: g_m and I_{DCIV} variations under hot carrier stress conditions with $V_g@I_{b,max}$ and $V_g=V_d$ were compared. For n-MOS, the worst case is $V_g@I_{b,max}$ for long channel devices and $V_g=V_d$ for short channel devices, while for p-MOS, all devices show the worst degradation at $V_g=V_d$. The g_m dependence on ΔN_{it} (ΔI_{DCIV}) was also monitored. The discrepancy between short and long channel devices can be attributed to the different ratio of channel to S/D resistance R_{CH}/R_{SD}.

Negative Bias Temperature Instability (NBTI) for p-MOS: NBTI in p-MOS has been suggested as the dominant factor for CMOS reliability[4]. We have observed a very interesting phenomenon of NBTI during a "dynamic" stressing. When an electric field of opposite polarity is applied during NBTI stressing, a reduction of ΔN_{it} is observed. This is interpreted by the interaction between N_{it} and hydrogen species. During negative biasing, the hydrogen is released from Si-H bond at the SiO_2/Si interface, moving towards the gate electrode and resulting in ΔN_{it}. When the bias polarity is reversed, the hydrogen is driven back to the SiO_2/Si interface under the applied electric field and passivates the Si dangling bond, resulting in ΔN_{it} deduction. We have shown that the "electrical annealing" of interface states can be very significant for p-MOS operating in a CMOS inverter, and hence the device lifetime under such "dynamic" NBTI stress can be much longer than that projected under the conventional "static" NBTI stress.

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