Electrical Properties and Reliability of Silicon Nitride Gate Dielectrics Formed by Various Process and Annealing

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The thickness of conventional thermal oxide in MOS device is intrinsically limited because of its severe leakage current. Gate dielectrics with higher dielectric constants (k) must be considered, which are physically thicker while electrically equivalent to ultra-thin thermal oxide. However, the electrical properties and reliability of high-k gate dielectrics are not satisfactory. Si_3N_4 formed by a JVD appears to be very favorable [1], which is not commercially available yet. Fortunately ultra thin Si_3N_4 formed by CVD and suitable annealing is demonstrated to be promising for gate dielectric of MOS devices [2]. Another report shows that oxidized silicon nitride gate dielectric is highly reliable for MOSFET [3]. It's recently shown that ultrathin oxynitride dielectrics formed by NH_3 nitridation is robust for reliability concerns [4]. Thus electrical properties and reliability of Si_3N_4 gate dielectrics deserves to explore further. Silicon nitrides formed by various methods and following annealing treatments are particularly investigated in this work.

Si_3N_4 dielectric was formed by a deposition in NH_3/SiH_2Cl_2 at 720 ℃ by LPCVD (Group I: Nit) or a thermal nitridation in NH_3 at 800 ℃(Group II: NH_3 Nit). Then rapid-thermal-annealing treatments were performed in N_2O by one-step annealing (O) and two-step annealing (T), respectively. The symbols for all experimental samples are listed as follows. Group I; **TR1**: Nit 20Å + N_2O 850 ℃ 15s + N_2O 800 ℃ 15s; **TR2**: N_2O 900 ℃ 20s + Nit 20Å + N_2O 850 ℃ 15s + N_2O 800 ℃ 15s ; **OR1**: N_2O 900 ℃ 20s + Nit 20Å + N_2O 850 ℃ 30s; **OR2**: N_2O 900 ℃ 20s + Nit 20Å + N_2O 800 ℃. Group II; **TR5**: NH_3 Nit 20Å + N_2O 850 ℃ 15s + N_2O 800 ℃ 15s; **TR6**: N_2O 900 ℃ 20s + NH_3 Nit 20Å + N_2O 850 ℃ 15s + N_2O 800 ℃ 15s; **OR5**: N_2O 900 ℃ 20s + NH_3 Nit 20Å + N_2O 850 ℃ 30s; **OR6**: N_2O 900 ℃ 20s + NH_3 Nit 20Å + N_2O 800 ℃ 30s. Physical thickness of Si_3N_4 films were measured by ellipsometry and were confirmed by capacitance-voltage method (k=5.4).

Figure 1 shows the maximum transconductance Gm of MOSFETs for group I (TR1, Nit) and group II (TR5, NH_3 Nit). Since the Gm of TR5 sample is clearly higher than that of TR1 one, Si_3N_4 gate dielectric formed by NH_3 nitridation is more advantageous than that by LPCVD. For TR1 sample, the lower mobility can be due to the higher interface trap density, which is caused by the lots of defects and interfacial strain induced during CVD. On the other for TR5 sample formed by NH_3 nitridation, the high nitrogen concentration and low defect at the interface result in a higher mobility [4].

Figure 2 shows the hot-carrier-induced maximum transconductance degradation (ΔGm/Gm) for MOSFET with Si_3N_4 gate dielectric treated by one-step annealing (OR5 and OR6) and two-step annealing (TR5 and TR6), respectively. Devices with two-step annealing have apparently smaller hot-carrier induced transconductance degradation than those with one-step annealing. The defects and interface strain can be reduced by the first oxidation. And the second oxidation in this two-step annealing may minimize the stress and defect at poly-Si/ Si_3N_4 interface. Although the oxidized silicon nitride gate dielectric is helpful for its reliability improvement [3], its better oxidation conditions are clearly important and need further detailed experiments for optimization. Regarding to the hot-carrier reliability comparison between group I (Nit) and group II (NH_3 Nit), a better performance for the former is found and is not shown here. A worse initial Gm and better reliability for group I (Nit) as compared with group II (NH_3 Nit) indicates a tradeoff for these considerations.

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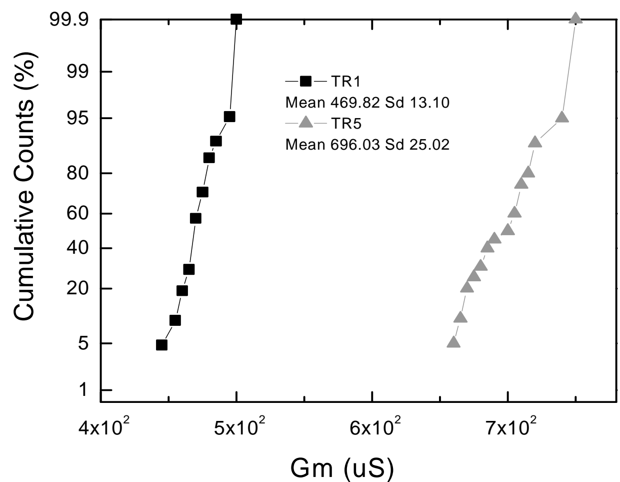

Fig. 1 Maximum transconductance Gm for group I (TR1, Nit) and group II (TR5, NH_3 Nit).

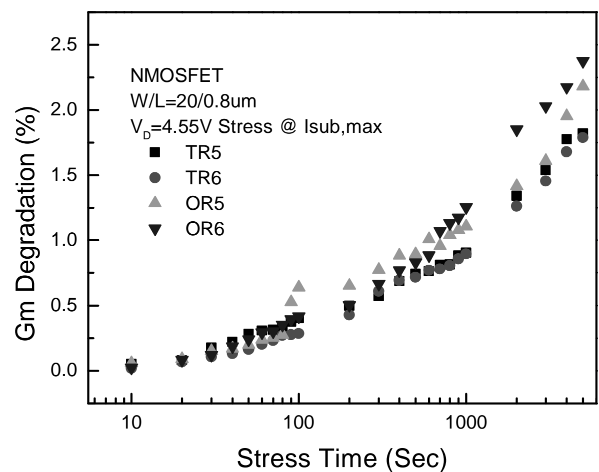

Fig. 2 Hot-carrier-induced maximum transconductance degradation (ΔGm/Gm) for MOSFET with Si_3N_4 gate dielectric treated by one-step annealing (OR5 and OR6) and two-step annealing (TR5 and TR6).