Predictive Simulation of Void Formation during the Deposition of Silicon Nitride and Silicon Dioxide Films

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INTRODUCTION AND MOTIVATION

In backend processes for memory cells ILD (interlevel dielectric) materials and processes result in void formation during gap fill. This approach lowers the overall k-value of a given metal layer and is economically advantageous. The impact of the voids on the total capacitive load is tremendous.

In order to provide predictive simulations of the overall capacitance, the shape and positions of the voids must be simulated accurately.

SIMULATION OF SURFACE EVOLUTION

The topography simulator ELSA (enhanced level set applications) has been developed for process simulations in the area of semiconductor manufacturing [1, 3]. Its main features are an efficient and precise level set algorithm including narrow banding and extending the speed function and a surface coarsening algorithm which reduces the computational effort significantly while ensuring high resolution in critical areas.

Test structures of interconnect lines of memory cells were fabricated and several SEM images thereof were used to validate the corresponding simulations. For metal lines 1 and 2 the deposition of silicon dioxide films from TEOS was considered and for metal line 3 the deposition of silicon nitride was simulated. The detail in Figure 1 shows metal 2 and 3 layers. The test structures contain trenches of different widths, and the influence of the width is precisely reproduced in the simulations.

The deposition of silicon nitride films was performed by PECVD from Silane and NH_3. For modeling the main reaction path we use $SiH_4 + NH_3 \rightarrow SiNH + 3H_2$ as the essential reaction [2, 4]. The path of the species above the wafer surface is tracked in radiosity simulations where reflection happens in a luminescent manner.

An example of void formation after silicon nitride deposition is shown in Figure 2. The shape and position of the void is reproduced correctly in the simulation.

CONCLUSION

The shape and position of voids in silicon dioxide and nitride films occuring in backend manufacturing processes are simulated accurately. The voids determine the capacitance of the interconnect lines, which is crucial for the performance of the final memory cell.

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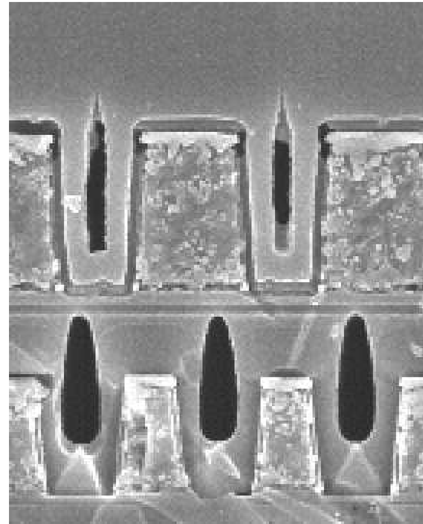

Figure 1

SEM image of a test structure with trenches of different widths. This detail shows metal 2 and 3 layers of the interconnect structure of a memory cell. In the upper row (M3 layer) the trenches are about 0.45μm wide and a nitride film was deposited. In the lower row (M2 layer) silicon dioxide was deposited from TEOS.

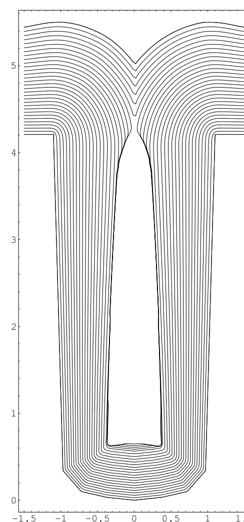

Figure 2

Simulation of void formation as shown in the metal 3 layer in Figure 1. Here a level set grid of $80 \cdot 120$ points was used.