

DIRECT-WRITE DEPOSITION OF SILICON OXIDE - THE EXPRESS LANE TOWARDS PATTERNED THIN FILMS

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Modeling of novel microelectronic devices, prototyping of microelectromechanical systems, modifications of chip interconnections, rapid wiring of test vehicles, remedy of defective circuitry, the development of new 3-dimensional designs and repair of photomasks are all issues where a reliable, rapid prototyping technique is long sought for flexible research and quick damage relief. Silicon oxide and silicon nitride holds the dominant position as dielectric in all previously described microelectronic devices relying on the utilization of metal and insulator structures. The prevalent structuring method for dielectric thin films is optical lithography. For mass production lithography remains unmatched in high throughput and economical value. However, this approach is less desirable for rapid prototyping - in research as well as for repair - since it requires extensive planning of the photomask design in advance. Furthermore, several process steps including formation of homogeneous dielectric films, photoresist processing and, etching of the dielectric are typically required to fabricate the demanded structure. An alternative method for the direct deposition of completely structured silicon oxide on any substrate surface is proposed. Direct-write deposition is a maskless technique that allows to deposit arbitrary structures of material within a single process step. Utilizing a focused particle beam to initiate a locally confined chemical vapor deposition (CVD) also 3-dimensional structures of silicon oxide can be fabricated (Fig. 1). Deposition of structures with a feature size down to 200 nm is shown to be feasible.

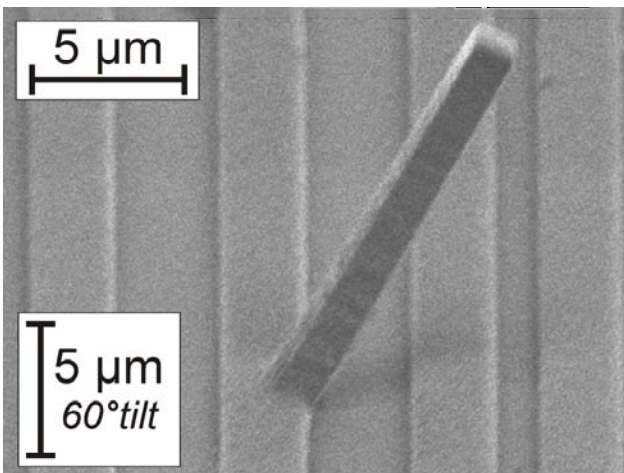


Figure 1. A 1x1 μm pillar of silicon oxide deposited at a 30° tilt angle to the surface deposited by FIB-CVD.

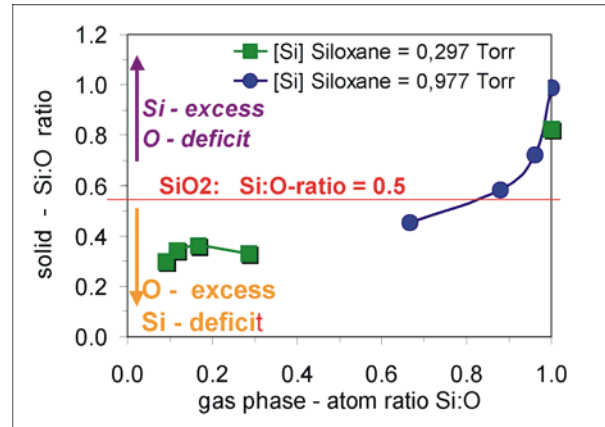


Figure 2. Composition of deposited silicon oxide in dependence on gas composition offered during CVD.

This work focuses on the fundamental aspects of the deposition of silicon oxide from a binary mixture of the precursor substances tetramethylcyclotetrasiloxane (TMTCS) and oxygen [1]. Using dosing valves the composition of the gas mixture could be varied. The gaseous precursors were introduced to the sample surface via a micro-nozzle system. For the focused particle beam a vacuum system with a base pressure of 10^{-6} mbar has to be used. The local chemical vapor deposition was initiated by a focused particle beam with a focus spot down below 10 nm that was scanned over the designated areas where material deposition was desired [2]. The acceleration voltage of the Ga^+ beam was varied between 10 and 50 keV acceleration voltage.

Electrical properties have been tested employing capacitor test vehicles revealing favorable insulating properties for microelectronic applications in interconnect technology. Due to the atomic intermixing by the high energetic ions causing an interface layer of up to 100 nm a minimum layer thickness of the FIB-deposited silicon oxide is required in order to guarantee good insulating properties. The thickness of this interface layer has been experimentally confirmed by cross-sectional images obtained with transmission electron microscopy (TEM) and also correlates nicely with results from simulation. A depth profile of the chemical composition of the deposited material has been measured by secondary ion mass spectroscopy (SIMS) and shows a homogeneous composition of the deposited material but also verifies the intermixing layer at the interface. Alternative deposition strategies for reducing as well as totally eliminating the atomic intermixing at the interface will be discussed.

The deposition process for silicon oxide has been optimized. Extensive data on the influence of the gas phase composition and total pressure on the chemical composition are presented (Fig. 2). Effects on surface morphology of the deposited layers have been investigated by atomic force microscopy (AFM) and a strong influence of scanning parameters such as pixel spacing and scan speed are observed. Based on the fundamental findings potential applications of this versatile rapid fabrication technology are assessed. Test prototypes of 3-dimensional devices and applications in interconnect technology are presented.

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[1] K. Edinger, J. Melngailis and J. Orloff, *J. Vac. Sci. Technol.*, **B 16(6)**, 3311 (1998)

[2] S. Matsui and Y. Ochiai, *Nanotechnology*, **7(3)**, 247 (1996)