Plasma damage in ultra-thin gate oxide induced by dielectric deposition processes: an overview on main mechanisms and characterization techniques

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INTRODUCTION

Plasma dielectric deposition processes are essential for the development of advanced CMOS technologies, because of their gap-filling properties and their low thermal budget. However, plasma induced damage due to antenna effects are still a main issue for the devices reliability. In this paper, we will identify a plasma non-uniformity as the main antenna effects cause on two different CVD tools: we believe that this charging cause is one of the main antenna mechanisms in copper back-end of lines processes. Our discussion will be supported by original experimental results based on a direct plasma characterization technique which shows a good correlation with the MOS devices induced damage. We will next propose different process solutions to reduce the damage. In a second part, we will focus on the characterization of the induced defects in the gate oxide: different techniques will be presented, and finally the evolution of the damage with the gate oxide thickness will be discussed.

EXPERIMENTAL

An ECR-CVD tool (high density plasma) and a PECVD tool are studied in this paper: the deposited dielectric layers are TEOS, silane, PSG films. CHARM-2® wafers have been used to measure the floating antenna voltage during the CVD process. Gate oxide induced damage is evaluated on CMOS structures with different poly and metal comb antennas. Gate oxide thickness is scaled from 5 to 1.5nm.

ANTENNA EFFECTS IN CVD PLASMA PROCESSES

An ECR-CVD tool was identified as the main charging source on a 0.25µm technology, Fig. 1a. The negative antenna voltages mapping (Fig.1b) recorded by a CHARM-2® wafer shows a good correlation with the antenna devices gate leakage and the oxide sputter rate mappings. Thus, a plasma non-uniformity is here the main origin of the antenna voltage and the induced damage on devices. The cause of this non-uniformity and the shape of the voltage mapping will be discussed.

REDUCTION OF DAMAGE

The first way to reduce the damage induced by an high density plasma source is to reduce the plasma density, by decreasing the plasma power source (Fig.2a). This allows to minimize the charging current. Another solution is to increase the process pressure, which allows to reduce the electron temperature and to optimize the plasma uniformity: antenna voltage values can hence be decreased, as shows the Fig. 2b. Others alternatives as decreasing the process temperature or increasing the gate oxide immunity against damage will be proposed in the paper.

IMPACT ON THE GATE OXIDE RELIABILITY

Different methods to evaluate the charging damage are presented: impact on the charge-to-breakdown of the device, gate leakage after a short voltage stress (Fig.3). Finally, we show that the plasma induced damage tends to decrease on ultra-thin gate oxide devices, because of the tunneling gate current which allows a charge evacuation from the antenna to the substrate without degradation.

CONCLUSION

Plasma damage induced by CVD processes are investigated in this paper. We focus on antenna effects due to a plasma non-uniformity, showing both antenna structures results and direct antenna voltage measurements. Process solutions to damage are presented. Finally, the impact on the gate oxide quality and the damage evolution with the gate oxide thickness are also investigated.

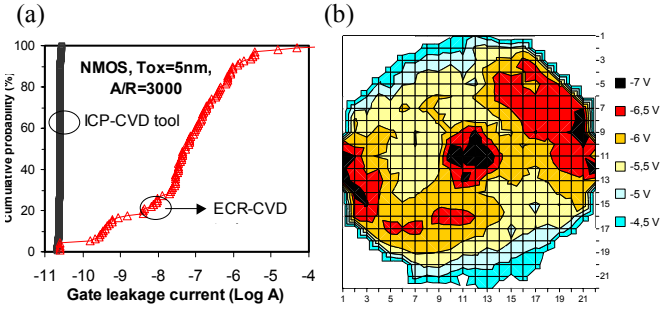

Fig. 1 (a)-Metal antenna structure degradation vs. the CVD tool. (b)- Negative antenna voltage in ECR-CVD tool.

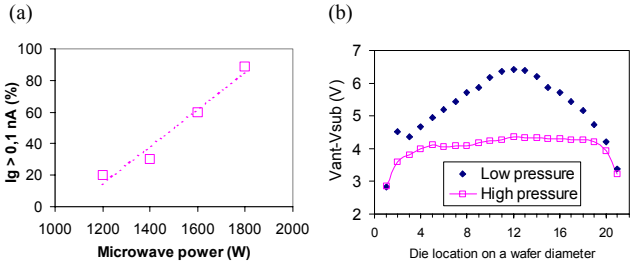

Fig. 2 (a) Charging degradation vs. microwave power in a ECR-CVD tool. (b) Positive antenna voltage vs. the process pressure in a PECVD tool.

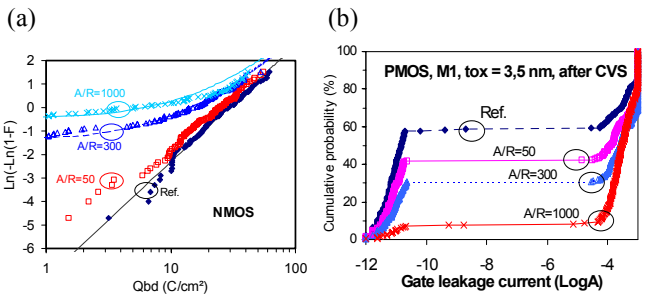

Fig.3 CVD charging impact on Qbd results (a) and gate leakage after a voltage stress (b). Tox =3.5nm.