Scaling Issues for Advanced SOI Devices: Gate Oxide Tunneling, Thin Buried Oxide, and Ultra-Thin Films

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Aggressive scaling of the gate oxide thickness and migration to ultra-thin Silicon On Insulator (SOI) transistors are necessary moves to face the International Technological Roadmap for Semiconductors (ITRS) constraints. In this paper, we present the future trends and address the critical issues related to the miniaturization of SOI MOSFETs. The scaling of the gate oxide, buried oxide, and silicon film is discussed based on extensive measurements and simulations. Most devices have been fabricated with advanced CMOS technology at LETI (Grenoble) and STMicroelectronics (Crolles) on Unibond material from SOITEC (Bernin).

Gate oxide. The development of ultra-thin oxides (sub-2.0 nm) results in enhanced direct gate-tunneling currents that affect the device performances in terms of power consumption and reliability. In Partially Depleted (PD) SOI devices, a direct consequence is the modification of the body-voltage and related floating-body effects. Such Gate-Induced Floating-Body Effects (GIFBE) are responsible for a kink in $I_D(V_G)$ characteristics and an outstanding second peak in transconductance. The influence of the gate-to-body current on the static characteristics is examined as a function of gate dimensions and measurement setup. It is also shown that the tunneling current can suppress the usual transient effects observed in SOI transistors (drain current undershoot or overshoot). This impacts on the history effects and overall performance of fast-switching SOI circuits. Finally, we demonstrate that GIFBE causes a low-frequency excess noise, the parameters of which are systematically investigated.

Buried oxide. Most advantages of the SOI devices result from the presence of the buried oxide (BOX): full vertical isolation, reduced leakage current and parasitic capacitances. The development of future generations of SOI circuits will require a rather thin BOX (50 nm or even less) in order to improve short-channel effects and self-heating. The aim of this section is two-fold. Firstly, the properties of recently developed SOI wafers with variable thin BOX are presented; the results have been obtained with the pseudo-MOSFET characterization technique. Secondly, the short-channel effects induced by the field penetration through the BOX and the substrate (fringing fields) are analyzed using simulations as well as experimental data. The guidelines for device optimization are discussed.

Silicon film. Fully Depleted (FD) SOI transistors with ultra-thin body (relaxed or strained) and/or double-gate architecture are the best candidates for further MOS scaling beyond the 10 nm barrier. Film thinning is extremely beneficial in terms of electrostatic control but also causes a number of interesting coupling effects to occur. We compare devices with body thickness from 5 to 15 nm and gate lengths down to 50 nm. The strong coupling between the front and back channels of single-gate MOSFETs is used to emulate pseudo double-gate transistors. We discuss the biasing conditions for optimum performance achieved by operation in volume-inversion mode.