Atomic, Electronic Structures and Charge Transport Mechanism in Silicon Nitride of Different Composition

Vladimir A. Gritsenko, Kamil A. Nasyrov[1]

Institute of Semiconductor Physics, 630090, Novosibirsk, Russia (e-mail: grits@isp.nsc.ru)
[1]Institute of Automation and Electrometry 630090, Novosibirsk, Russia

Silicon nitride of different composition (Si_3N_4, SiN_x, SiO_xN_y) has been one of the key dielectrics in modern devices. The carrier localization property in Si_3N_4 and SiN_x is now proposed for the design of terabit scale silicon-oxide-nitride-oxide-silicon (SONOS) EEPROM. The trap properties and the charge transport mechanism in this material are the most important concerns for this application. On the other hand, the conventional thermal oxide will soon be replaced by oxynitride (SiN_xO_y) in the giga-scale MOS devices and the aforementioned properties are also important. This paper presents a systematic study on the atomic structure, trap electronic structure, and charge transport mechanism in SiN_xO_y and SiN_x with different composition.

The atomic structures of the dielectric defects are governed by the short-range order in dielectric film. The short-range order in SiO_xN_y can be described by the Mott rule. According to this rule the Si atom is coordinated by four N/O atoms, N and O atoms are coordinated by three and two Si atoms, respectively. The bonding in SiO_xN_y is described by random bonding (RB) model. According to the RB model, SiO_xN_y is composed of five types of tetrahedra $SiO_\nu N_{4-\nu}$, where ν = 0, 1, 2, 3, and 4. For SiN_x, the bonding cannot be described by RB model and there are large scale potential fluctuations in SiN_x because of the non-uniform chemical composition.

To study the trap electronic structure, quantum-chemical simulation was performed. We found that single neutral diamagnetic Si-Si bond, or small Si clusters are amphoteric traps responsible for electron and hole localization in Si_3N_4. However, there is no ESR signal after electron/hole localization in Si_3N_4. This effect can be explained by Wigner crystallization of localized carriers. Due to Coulomb repulsing localized carriers create Wigner quasi-periodic glass in nitride. Localized electrons are pairing through empty trap-assisted resonance tunneling. With quantum chemical simulation we also found that the two-fold coordinated nitrogen atom (=N•) is an electron trap in Si_3N_4 and SiO_xN_y.

Charge transport mechanism was also studied in this work. The Frenkel effect is the widely accepted model for trap ionization. However, our experiments on the charge transport in Si_3N_4 show that the escape frequency with Frenkel model is about 10^7 sec^{-1}, and is unreasonable low. In addition, the effective tunnel electron mass ($m^* \approx 4m_e$) obtained by experiment data fitting within this model is abnormally large and is of one order of magnitude large than other experiment. With this connection, a new model is developed to explain the charge transport in Si_3N_4. We propose that the trap ionization is due to multi-phonon process. The multi-phonon trap ionization model is in a good quantitative agreement with experiment.

Silicon-oxide-nitride-silicon (SONOS) EEPROM is promising for design of giga- and terabit memory. Usually SiO_2 is used as a top oxide in a conventional SONOS. Since SiO_2 has a low dielectric permittivity ε=3.9 in comparison with Si_3N_4 (ε=7.5) the electric field in top oxide is about two time larger, than in nitride. Therefore, for scaled SONOS device with comparable thickness of nitride and SiO_2 top oxide, a remarkable part of applied voltage drops on the top oxide during write/erase (W/E) programming. This undesirable voltage drop and, consequently, the total applied voltage can be decreased by replacing SiO_2 by high-k dielectric. We simulate the W/E processes in SONOS with high-k dielectrics Al_2O_3 (ε=9) and ZrO_2 (ε=25) as a top blocking dielectric. One-dimensional two bands model of charge transport is used, which takes into account Shockley-Reed-Hall statistics for trap population, continuity and Poisson equation. This model considers carrier double injection from silicon substrate and from poly-Si gate. The simulation shows that SONOS with high-k dielectric as a top oxide has the following advantages in comparison with conventional SONOS device:

1) For the fixed SONOS geometry the W/E programming voltage decreases.
2) The using high-k dielectric for fixed W/E voltage speeds up W/E process.
3) For the fixed time of W/E process and voltage the application of high-k dielectrics as a top dielectric allows to use thicker bottom SiO_2 layer, which can provide the larger retention time.