MOSFET Degradation with Reverse Biased Source and Drain During High-Field Injection through Thin Gate Oxide

B. Patel, R. K. Jarwal and D. Misra
Department of Electrical and Computer Engineering
New Jersey Institute of Technology, University Heights
Newark, NJ 07102

With continued scaling of MOSFETs the reliability of thin gate oxides is becoming increasingly important. Degradation issues due to fabrication technology may result in misinterpretation unless the actual physical situation arising at source, drain, gate and substrate of a transistor during processing is understood. It has been shown recently that the energy of hot electrons relative to Fermi level position at anode/cathode interface controls the degradation [6]. This degradation is prominent in plasma processing results due to wafers charging where similar high-field injection occurs [2]. Depending upon the polarity of plasma potential relative to wafer the high-field electron injection process could be from gate or substrate. It has been shown that damage for substrate injection is more pronounced [3]. The voltages developed at source and drain junctions, depending upon polarity relative to the substrate cause the source/drain (S/D) junctions to be forward biased or reverse biased [4]. Keeping in view this type of physical situation arising at the source and drain junctions, this paper reports the effects of reverse biased potential at source and drain junctions of a NMOSFET during high-field injection for substrate injection and its impact on device parameters.

For the present study n-MOS transistors (gate length = 0.35μm; oxide thickness = 6nm) were processed using 0.25μm technology. A forming gas annealing of the transistors was performed before any measurement. Transistors were then subjected to about 400mA/cm^2 constant current stress and 10V constant voltage stress for 3 seconds using substrate injection mode. Threshold voltage V_t values measured before stress were quite uniform. Threshold voltage shift, hot carrier stress and breakdown measurement of the transistors were measured.

The variation of $\Delta V_t/V_t$ as a function of reverse biased voltage at source and drain junctions for constant voltage stress and constant current stress for substrate injection modes is shown in Fig. 1. It can be noticed that the nature of threshold voltage degradation is similar for both constant current and constant voltage stresses. The threshold voltage shift increases gradually with reverse biased voltage. Experimentally observed threshold voltage prior to stress is lower than threshold voltage after stress indicates dominant electron trapping. Since the device is in strong inversion an increase in reverse biased voltage will form the channel in the center of the device due to the depletion regions of source and drain junctions. This enhances the current density during high-field injection damaging the oxide further. Co-relation with hot carrier effects in these devices will be explored.

In summary, degradation to threshold voltage V_t of n-channel MOSFETs due to reverse biased potential at source and drain junctions during high-field electron injection was observed. Stress induced V_t shifts showed a dependence on the reverse biased voltage during substrate injection.

ACKNOWLEDGEMENT

This work supported by a grant from National Science Foundation award number 0140584.

REFERENCES

[1] D.J. DiMaria, Appl. Phys. Lett. vol.68, p.3004, 1996.
[2] D. Misra, IEEE Trans. On Electron devices,
[3] D.Misra and K.P.Cheung, Semicond. Sci. Technol. vol. 13, p.529, 1998.

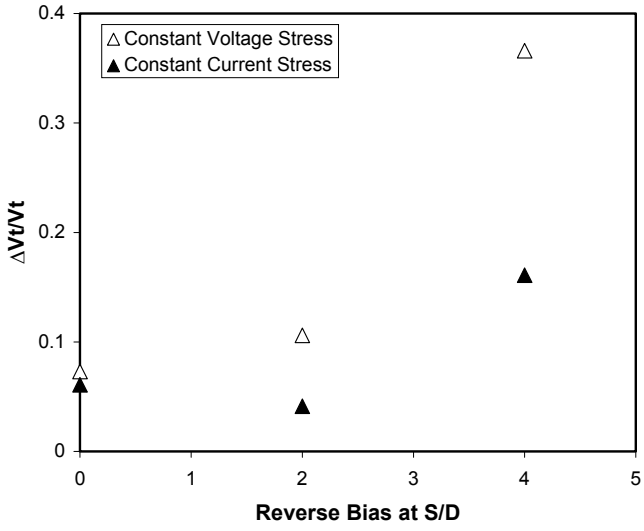

Fig. 1. $\Delta V_t/V_t$ due to voltage and current stress as a function of reverse biased voltage for substrate injection case.