Recovery and reversibility of electrical instabilities in double-layer dielectrics

Serge Evseev and Antonio Cacciato

Philips Semiconductors, Q&AS
Gerstweg 2, 6534 AE Nijmegen, The Netherlands
Phone: +31-24-353-2007, Fax: +31-24-353-3323
E-mail: serge.evseev@philips.com

Electrical instabilities in double-layer dielectric (DLD) films are studied as a function of measurement conditions by means of Bias-Temperature (BT) stress in parasitic Metal-Insulator-Semiconductor Field-Effect Transistor (MIS-FET). It is shown that the threshold voltage shift (ΔV_T) is larger if the conductance difference between two insulating layers is higher and that the ΔV_T is recoverable within several seconds. The effect is found to be reversible and its polarity can be altered by changing the polarity of the stress voltage.

In modern ULSI technology, Chemical Vapor Deposited Oxides (CVD-SiO_2) and Tetraethyl Orthosilicate (TEOS) films are well accepted as intermetal dielectrics (IMD) to electrically isolate metal layers in multilevel-interconnect systems. A second insulating layer such as Aluminum oxide (Al_2O_3), Phosphosilicate glass (PSG), or Plasma Enhanced CVD silicon nitride (PECVD-Si_3N_4) is frequently deposited on top of the CVD-SiO_2 film to prevent mobile ion contamination. Injection and trapping of the electric charge in DLD films may cause electrical instabilities in parasitic devices [1, 2]. In this work, we explore the nature of the ΔV_T shift in DLD's and demonstrate that the shift is recoverable and reversible.

An N-well MIS-FET consists of source and drain terminals, which are situated symmetrically with respect to the 700 nm thick Locally Oxidized Silicon (LOCOS) isolation with the DLD film on top. The DLD layer is formed by combining two of the following dielectrics: 900 nm Plasma Enhanced Chemical Vapor Deposited (PECVD) silicon nitride (Si_3N_4); 800 nm PECVD oxide (SiO_2); 650 nm Boron Phosphorus Tetraethyl Orthosilicate film (BPTEOS); 550 nm Low Pressure Chemical Vapor Deposited (LPCVD) Tetraethyl Orthosilicate film (TEOS). The following DLD's were formed with an aluminum gate on top: Si_3N_4/BPTEOS, Si_3N_4/TEOS, and SiO_2/BPTEOS. MIS-FET's were stressed at gate biases (V_{BIAS}) between -100 and 100 V, temperatures between 150 and 300 ºC, and stress times between 3 and 3333 s. From the drain current versus gate voltage characteristics (I_{DS}-V_{GS}) the threshold voltage shift defined as $\Delta V_T = V_{AFTER} - V_{BEFORE}$ was calculated. V_{AFTER} and V_{BEFORE} represent the voltages recorded before and after the gate stress, corresponding to a drain current $I_{DS} = 10^{-5}$ A.

The results showed that the largest ΔV_T shift was observed for the Si_3N_4/BPTEOS and it decreases for the Si_3N_4/TEOS and was the smallest for the SiO_2/BPTEOS. For example, at 250 ºC, 33s, –100 V BT stress, ΔV_T is equal to 13.27 V, 4.76 V, and 2.26 V for Si_3N_4/BPTEOS, Si_3N_4/TEOS, and SiO_2/BPTEOS DLD's, respectively. The same trend was also found for different voltages and stress times. Direct current-voltage measurements show that a correlation exists between the conductivity of the dielectrics and ΔV_T. It was found that the Si_3N_4 has the largest conduction current while the TEOS layer has current three orders of magnitude lower than Si_3N_4, whereas only a small difference is observed between BPTEOS and SiO_2. It can therefore be concluded that the largest ΔV_T (Si_3N_4/BPTEOS) corresponds to the largest difference in conduction currents. The medium voltage shift (Si_3N_4/TEOS) corresponds to the medium difference in conduction currents and negligible voltage shift (SiO_2/BPTEOS) corresponds to almost identical conduction currents.

The reversibility of the ΔV_T in the case of Si_3N_4/BPTEOS DLD film was also studied. Five stresses of either polarity were performed one after the other on the same gate at 200 °C for 333 s. Each stress was carried out at a different stress voltage (V_{BIAS}). Ten stress voltages varied from –100 V up to 100 V. The ΔV_T was measured after each stress. It was found that ΔV_T increases (in absolute value) from -0.8 V to –28.3 V if V_{BIAS} was increased from 8 V to 100 V. At this point, if the polarity of V_{BIAS} was changed from 100 V to –100 V, ΔV_T abruptly changed from –28.3 V to 15.3 V. It was possible to reproduce the effect several times, still observing the same changes of ΔV_T within the measurement accuracy of the experiment.

Figure 1 shows the recovery of ΔV_T after stress in the case of the Si_3N_4/BPTEOS DLD film. It was found that after only 3 s ΔV_T voltages were recovered to 86%, after 33 s the voltages recovered to 92%, and after 333 s to 99% of their original values for -32 V, 250 °C, 33 s stresses. As can be derived from Figure 1 the recovery curve obeys a logarithmic dependence.

The reported instabilities are explained with accumulation of electric charge at the Si_3N_4/BPTEOS interface due to a conductance difference between two dielectrics and a first-order charge transfer model has been developed [2].

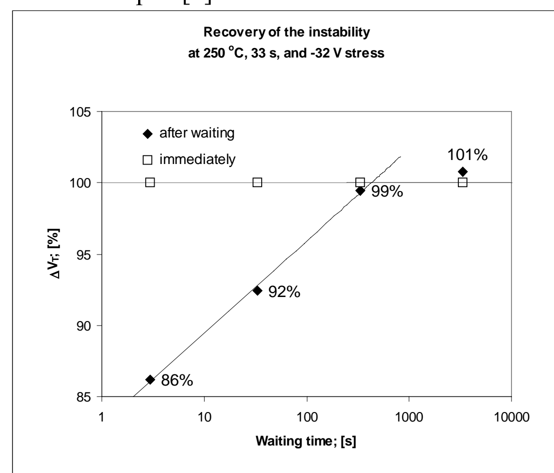

Figure 1 ΔV_T immediately vs. waiting time after the stress. Horizontal reference line corresponds to the voltage shift immediately after the stress.

The instabilities in double-layer dielectric films with different conductances represent a reliability hazard for electrical circuits at elevated temperatures and biases. Therefore, special care should be taken if double (or multiple) dielectric layers are used as intermetal or passivation dielectrics. However, the results indicate that the hazard is only present during BT stress because the voltage shift is completely recovered within several seconds after the stress is removed. The device should then return to its normal operating regime.

[1] G. Barbottin and A.V. Vapaille, *Instabilities in Silicon Devices*, Elsevier Science, Amsterdam, 1989, Chap. 16.

[2] S. Evseev, A. Cacciato, and J. van der Pol, *Conduction-related voltage instabilities in double-layer dielectric films*, J. Appl. Phys. Vol. 91 (9), 1 May (2002), pp. 6206-6208.