Electrodeposition of Through Chip Copper Plug for Three Dimensional Packaging (2)

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Through chip electrodes having high-aspect-ratio-vias (Fig. 1) are able to provide the shortest interconnection between chips, thereby reducing signal delay. For filling high-aspect-ratio-vias, copper electrodeposition was adopted because of good compatibility of copper to conventional multi layer interconnection in BEOL (back end of line process) of LSI [1, 2]. Previously we reported that filling vias with high aspect ratio, 10 μm in square and 70 μm in depth, used for through chip electrodes, was accomplished without void or seam in 12 hr of plating time [3]. With a optimzed electrodeposition condition by testing a series of electrodeposition conditions, perfect via filling of the electrode without overhang at via top was achieved by pulse reverse plating method as well as by increasing JGB concentration up to 20 mg/L in the plating bath, suggesting that bottom-up filling be markedly realized by adopting the above conditions. Yet, the plating time of 12 hr was not short enough to be used practically.

In this regard, for the purpose of accomplishing time-shortening with the use of a <u>commercially-available</u> bath and <u>specially-designed</u> ones, we are concerned with investigating copper pulse reverse plating to fill vias with the above-mentioned aspect ratio. We used the <u>commercially-available</u> bath containing $CuSO_4 \cdot 5H_2O$ and H_2SO_4 for basic bath, and PEG (polyethylene glycol), JGB (Janus Green B), SPS (Bis (3-sulfopropyl) disulfide) and HCl as additives. With this commercially-available bath of further optimized composition, electrodeposition time was shortened to 3.5 hr (Fig. 2) by adopting novel two-step electrodeposition method, i.e. by applying initial lower current of 2 mA/cm^2 for 2 hr and final higher current of 3 mA/cm^2 for 1.5 hr.

In the case of <u>specially-designed</u> baths, we firstly used four kinds of baths containing; (SPR A), (SPR B), (LEV A + SPR B) and (LEV B + SPR B). Here, SPR and LEV denotes suppressor and leveller, respectively. Baths containing SPR B showed better via filling abilities than others. Therefore, we chose LEV B as well as SPR B as DoE (Design of Experiment) parameters. With the partial help of a predictive model from DoE for electroplaitng time vs. addtives, we may optimize further the composition of specially-designed bath, in order to accomplish time-shortening of about 1.0 hr. Via-filling mechanism will be mentioned in the discussion section.

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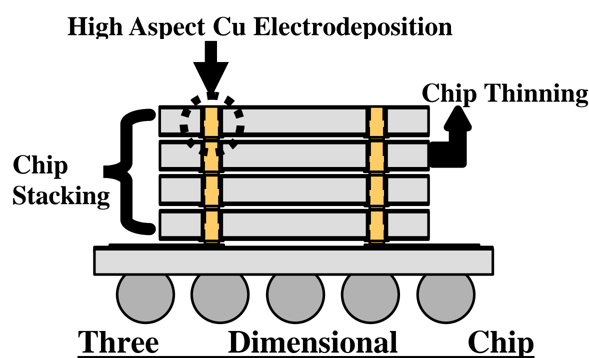

Figure 1. Schematic illustration of chip stacking for 3D packaging.

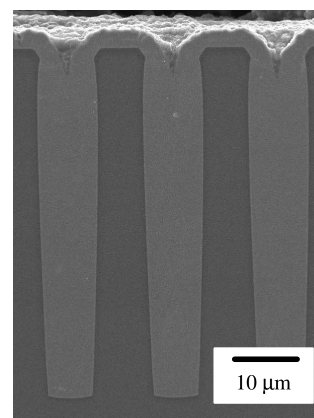

Figure 2. SEM photograph of completely-filled through chip electrodes with 10μm in square and 70μm in depth **<u>for 3.5 hr.</u>**