Stress management in IC manufacturing: µ-Raman Spectroscopy re-visited

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ABSTRACT

Developments in Integrated Circuits technology are primarily aiming at more complex and better performing circuitry while optimizing silicon real estate. To meet these ambitious targets, today, the IC industry continuous to shrink the critical dimensions of CMOS and Bipolar structures (180 – 65 nm) but also introduces various novel materials that may help to push the physical limits even further. While reduced feature size and novel materials help to improve the intrinsic characteristics of the IC, also new reliability problems show up that are related to more important stress levels generated in the structures.

Transistor isolation, nowadays, is realised by shallow and deep trenches in Si that are filled with dielectric material (Fig. 1). The sharply edged, rectangular structures and the thermal mismatch between Si and dielectric make that high 3-D stress components exist that may relax through the generation of silicon defects. Given the small device dimensions, the as such created defects can have a detrimental effect on device yield (Fig. 2) and thus, require utmost attention from process engineers.

In the process backend, the electrical wiring is realised in many Copper metal levels seperated by new intermetal dielectric materials (low-K dielectrics). Without appropriate stress engineering of the complete stack, the combination of new metal and isolation materials and reduced line width may again show extreme stress levels that can cause yield killing events such as material cracking, delamination or metal voiding.

To master above mentioned problems, developers turn more and more to physical characterisation methods such as Transmission Electron Microscopy (Fig. 3), X-ray techniques and Raman spectroscopy to characterise material properties, stress levels and stress induced defects.

In this presentation, the application of such techniques in avanced IC technology is illustrated and results are discussed. A special emphasis is given to µ-Raman spectroscopy applied to X-sectioned device structures. The impact of cleavage and milling of the silicon substrate on (3D) stress relaxation is demonstrated by µ-Raman spectroscopy, results that may put a different light on stress quantification using TEM based diffraction methods (CBED).

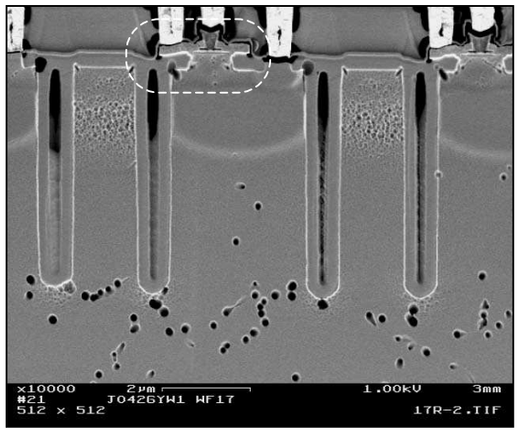

Figure 1. Bipolar transistors separated by Deep Trench Isolation (DTI). The active transistor area is indicated by the circle. Stress induced silicon dislocations are revealed primarily at the bottom part of the deep trenches but also near the transistor region.

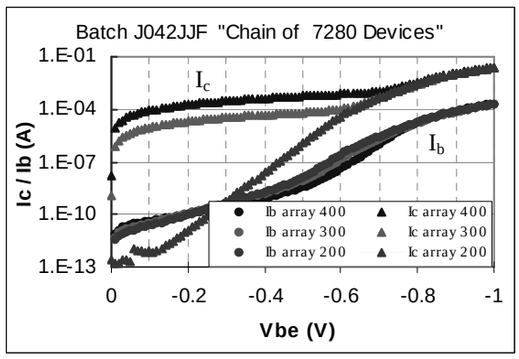

Figure 2. Gummel plot of an array of ~10000 Bipolar transistors isolated by Deep trenches (DTI) filled with different amounts of TEOS oxide and poly-crystalline silicon. Abnormal transistor characteristics (high leakage currents) are observed for the trenches that are filled with oxide rather than silicon (array 300 and array 400), i.e. for structures exhibiting the highest mechanical stress.

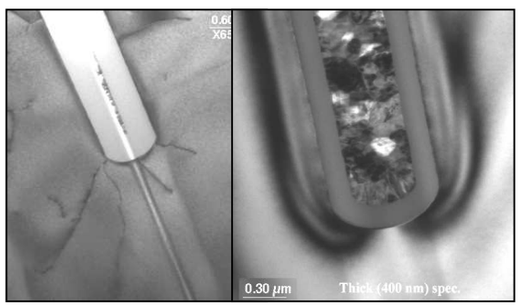

Figure 3. TEM analysis of DTI structures. Left: direct TEM observation of silicon dislocations around the trench bottom. Right: TEM diffraction image of same zone. The fringes around the trench bottom are indicative for high local stress level.