Two dimensional carrier profiling using scanning capacitance microscopy

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As emphasized in the International Technology Roadmap for Semiconductors (ITRS), two dimensional (2D) carrier profiling is one of the key elements in support of technology development. Sub-10 nm resolution, wide dynamic range (10^{16}-10^{20} at/cm^3) and good quantification accuracy (10%) are the most important points to be achieved. In the past years different promising analytical tools based on Atomic Force Microscopy (AFM) have emerged for carrier profiling, such as Scanning Capacitance Microscopy (SCM), Scanning Spreading Resistance Microscopy (SSRM) and Nanopotentiometry (NP). All these techniques use a small conductive probe that is scanned across a semiconductor surface while both the topography and an electrical signal (proportional to the local concentration) are acquired (fig. 1). Applied to the cross-section of a device, they enable 2D carrier profiling with high-resolution (10-30 nm). In this way, detailed studies of 2D dopant interactions and related parameters such as channel length, diffusion properties, junction position can be performed, whereas conventional (1D) techniques (such as SRP, SIMS) are not suitable anymore.

This work is focussed on SCM, where the measured capacitance can be related with the local carrier concentration. This technique can both be applied to Si-devices (fig. 2) as well as to III-V materials such as laser structures. The aim of this work is to make a state-of-the-art evaluation of the practicalities and limitations of SCM. With the aid of different examples the strong and weak points (reproducibility, spatial resolution, quantification accuracy,...) of the technique will be discussed.

One of the strong points of SCM is for example its high resolution (fig. 3). However several parameters such as tip size and oxide thickness play an important role for achieving this high resolution. One of the weaker points of SCM is its dependence on the applied voltage. When applying different dc-bias to the sample a movement of the pn-junction is measured (fig. 4). This raises the question at which voltage the correct junction position is measured. Since junction delineation is an important topic in semiconductor industry it is important to solve this problem. By using an extension of SCM – SCS - this problem can be partly solved.

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REFERENCES

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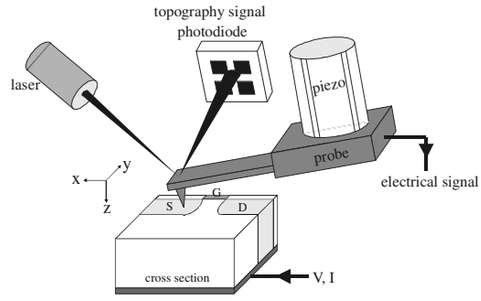

Figure 1 : Schematic drawing of the AFM principle. The reflected aser spot is on a probe, which is moving across the cross-section of a device, is inverted in the topography signal, while the probe measures an electrical signal which is related with the doping concentration under the probe.

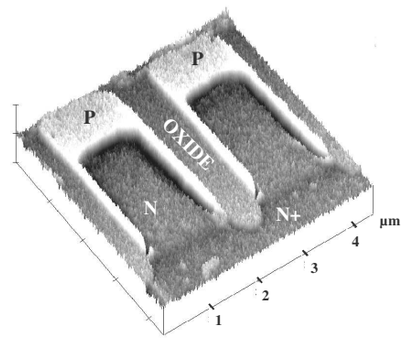

Figure 2 : Example of an SCM measurement of a vertical resurf diode [1]. The different doping areas can be distinguished with high accuracy. Study of the thin p-layer at the trench sidewall cannot be done with conventional 1D profiling techniques.

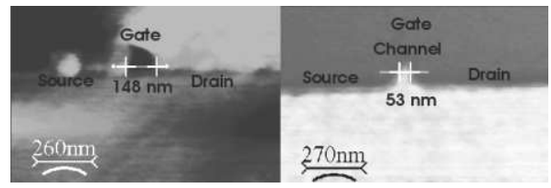

Figure 3 : SCM image of a 0.15 µm NMOS transistor. Left shows the topography with a 0.15 µm gate. Right shows the capacitance image. The channel length under the gate is measured with high resolution.

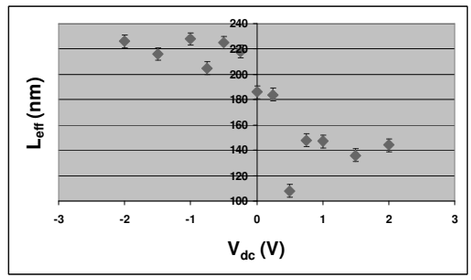

Figure 4 : Effective channel length of a 0.5 µm transistor measured at different biases with SCM. A movement of about 30nm/V is measured. The ideal dc-bias has to be determined to delineate the junction positions with high accuracy.