Novel Memory Concepts on SOI

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CMOS devices integrated on Silicon On Insulator (SOI) wafers are becoming widely accepted for high performance, low power, low voltage, high temperature, radiation hard or RF applications. Up to now standard active or passive devices were integrated on SOI substrates to address those applications. In the area of memory, standard SRAM, DRAM, or EEPROM cells have been integrated on SOI and can be used as on bulk.

More recently, Okhonin et al. [1,2] have proposed to exploit the floating body effects seen in SOI devices in order to realize a new memory cell, referred to as the 1T-DRAM. In this paper we will review the basic 1T-DRAM concept, discuss its performances and limitations and propose some extensions.

The 1T-DRAM memory cell is a real single transistor DRAM memory. No storage capacitor is needed. An excess of positive or negative charges in the body of an N or PMOS device is used to store the data states. These charges reduce or increase the transistor threshold voltage. The information is read by comparing the current *Id* of the selected cell to the current of a reference cell. As the information is reduced with time, this memory is still a dynamic memory and needs to be regularly refreshed.

Writing and reading the two states is illustrated in Figure 1 where well chosen writing conditions avoid static power dissipation during programming.

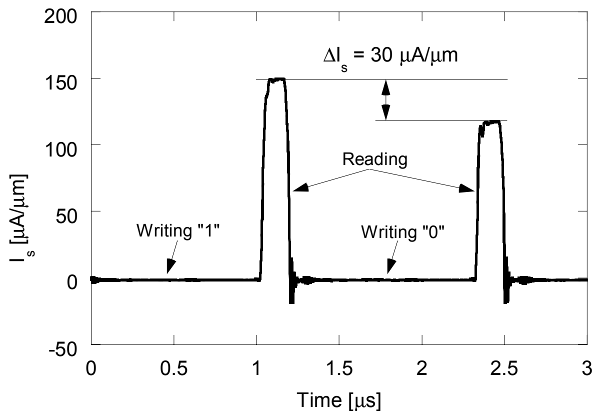

Figure 1: "1" and "0" states in 130 nm PD SOI NMOS devices with 100 nm Si. W/L = 10/0.13 µm.

The 1T-DRAM cell can be used for standalone or embedded memory applications to replace standalone or embedded DRAM or SRAM memories. Standalone 1T-DRAM allow a $4F^2$ cell area to be reached, while a 9 to 15 F^2 area is typical for embedded applications integrated in a logic process. These cell areas are typically 2 times smaller than their bulk counterparts.

A 1T-eDRAM has been laid out in typical logic technologies at the 130 and 90 nm rules. The circuit design exploits the fact that the read operation is non destructive to decode the columns prior to sensing. This allows to considerably reduce the number of sense amplifier when compared to regular DRAMs. The column decoding also suppresses the need of complex twisting schemes for the bit lines as the non decoded bit lines can shield and protect the signal on the decoded ones. A 1 Mbit eDRAM module is represented in the Figure 2. The cell and circuit area is summarized in the Table 1 for 130 and 90 nm rules and is compared to existing technologies.

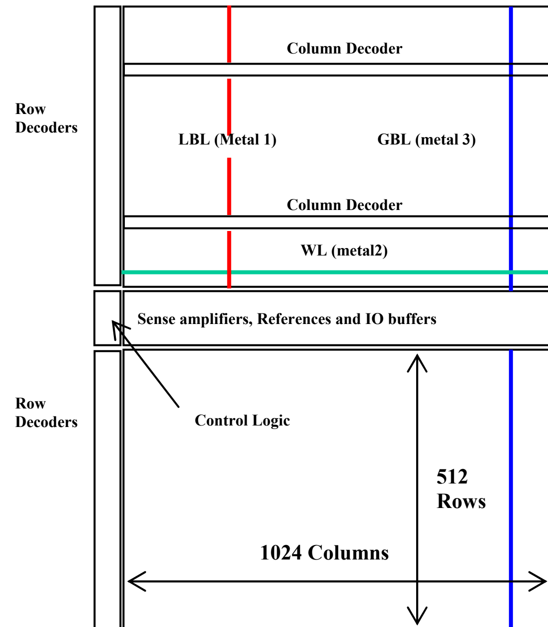

Figure 2: Block diagram of a 1 Mb eDRAM exploiting the 1T-DRAM concept.

Memory Type	Bit Cell (μm^2)	Macro (mm^2/Mb)	Area Factor	Technology	Speed	Active Power
6T-SRAM 130 nm	2.43	3.73	10.4	CMOS	Ultra fast	High
STC DRAM 130 nm	0.4	1.1	3	CMOS +6M	Slow	Medium
Planar DRAM 130 nm	1.1	1.9	5.3	CMOS	Fast	Low
1T-DRAM 130 nm	0.26	0.36	1	SOI CMOS	Fast	Ultra low
6T-SRAM 90 nm	< 1.25	< 1.9	9.5	CMOS	Ultra fast	High
STC DRAM 90 nm	0.2	0.6	3	CMOS +6M	Slow	Medium
Planar DRAM 90 nm	0.66	1.14	5.7	CMOS	Fast	Low
1T-DRAM 90 nm	0.13	< 0.2	1	SOI CMOS	Fast	Ultra low

Table 1: Embedded memory comparison for 130 nm and 90 nm logic technologies.

The 1T-DRAM cell allows eDRAM circuits to be 3 times smaller in area than conventional bulk eDRAMs or 10 times smaller than 6T-SRAMs. Extensions of this concept have been demonstrated on Si to fully depleted SOI devices and by simulation to double gate structures. We believe the shift of the mainstream technology to SOI will allow such new types of dense memory concepts to become widely accepted and will allow System On Chips (SOC) to flourish on SOI.

[1] S. Okhonin et al., Proc. Of the 2001 IEEE International SOI Conf., p.153, 2001.

[2] S. Okhonin et al., IEEE Electr. Dev. Lett. 23, p.85, 2002.