A Novel CMOS Memory Cell Architecture for Ultra-Low Power Applications operating up to 280°C

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Embedded SRAM appear as major static power dissipating block in Systems on Chip. This becomes even more true with supply voltages (V_{DD}) predicted to be as low as 0.4V in 2016. At such levels, static power might become dominant due to the reduction of threshold voltage (V_{th}) needed to maintain speed performances. We demonstrate a novel CMOS memory cell intended for ultra-low power (ULP) applications that can face this problem and work at very low V_{DD} as well as in elevated temperature conditions.

The architecture is based on a *new CMOS diode concept* [1] (fig.1). This ULP diode presents much smaller reverse current than the standard MOS diode and features a negative impedance region (fig. 1). Our *novel ULP memory cell* is obtained by connecting two reverse biased ULP diodes in series (fig. 2a). Two stable states appear, at "0" and "V_{DD}", in the plot of the current difference between the lower and the upper ULP diodes (D2 and D1) versus the voltage level at the memory node (V_{ram}) (fig. 2b). Subsequently, when a V_{ram} between 0 and $V_{DD}/2$ is imposed and then left floating, I_{D2}-I_{D1} is positive and eventually drives V_{ram} to "0". Reciprocally, when the imposed V_{ram} lies between $V_{DD}/2$ and V_{DD}, the cell current drives the floating memory node up to V_{DD}. Such architecture is therefore auto-regenerative for both logical levels "0" and "1". The spread and maximum value of the current peaks in figure 2b depend on device doping levels and temperature. Asymmetry in the threshold voltages of n- and p-MOSFETs of the diodes results in an increase of the regenerative current, thereby enlarging noise margins. A wider voltage range for the regeneration is also obtained when the temperature increases, allowing high temperature functionality of the cell.

In a stable logic state, the transistors of our cell are biased with low V_{ds} and negative gate to source voltages (V_{gs}) in very weak inversion, while V_{ds} is high and the minimum V_{gs} is 0 in a standard SRAM cell. This leads to an ultra low static consumption in comparison with standard SRAM. In practice the static current is equal to the junction leakage current of the transistors (defined as the minimum drain to source current for negative gate to source voltage).

The dynamic consumption is lowered as well due to the very low short-circuit current. At the middle point, both diodes are indeed strongly reverse biased leading to a very low current (fig. 1). The cell is intended to work at low supply voltage, as low as two times the diode voltage corresponding to the highest reverse current. It could therefore work down to 0.4V of supply voltage.

When considering the write operation speed, the intrinsic regenerative current of the cell can be neglected compared to the current driven by the access transistor. The latter and the memory capacitance thus define the speed performance. The memory capacitance is about the gate oxide capacitance of one MOS device of the diode only. The access transistor has to be designed such that his leakage current doesn't affect the content of the cell (e.g. using higher V_{th}). The read operation speed will not depend on the cell itself but on the read scheme and circuitry.

Diodes and memory cells were fabricated on a 2-µm fully depleted (FD) SOI CMOS process, on SmartCut UNIBOND wafers. The thicknesses of buried oxide, silicon film and gate oxide are 400, 80 and 31nm respectively. Both n- and p-MOSFET channels are boron implanted yielding inversion- and accumulation-mode operations respectively. ULP diode measurements demonstrated the expected behavior given by the simulations. High temperature characterization up to 300°C confirmed the spread and increase of the peak current in the reverse mode, compatible with correct ULP memory behavior.

Functionality of individual test ULP memory cells has been demonstrated up to 280°C. Static consumption was measured and appeared to be equal to the junction leakage current of the single transistors, up to the nA range only at very elevated temperature.

To conclude, the operation of a novel ultra-low power memory cell has been demonstrated in FD SOI CMOS technology. The architecture combines the self-regeneration property of a SRAM with the low memory node capacitance and low power consumption of a DRAM. It is furthermore intrinsically resistant to temperature elevations. Preliminary simulations with 0.12µm Partially-depleted SOI CMOS parameters demonstrated the feasibility of the ULP cell with short channel devices and confirmed the excellent power performances.

REFERENCES

[1] Patent H01L 27/092, "Ultra-low power basic blocks and their uses."

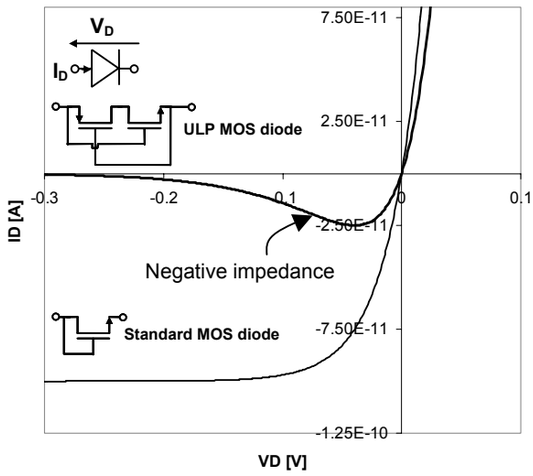

Fig. 1: Standard and ULP MOS diodes architectures and I-V simulated characteristics

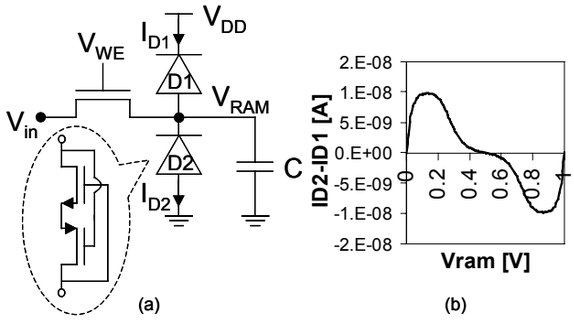

Fig. 2: (a) ULP memory (C represents the parasitic capacitance at memory node, not an additional capacitor); (b) Simulated current-voltage characteristic at V_{DD}=1V