Real Space Transfer Devices in SOI

Serge Luryi
State University of New York at Stony Brook
Stony Brook, NY 11794-2350 USA

Three-terminal real-space transfer (RST) devices employ charge injection of hot electrons over a potential barrier into an independently contacted second conducting layer.[1] The first conducting layer is the usual transistor channel, where electrons are heated by the source to drain field (Fig.1). The high RST injection is accompanied by a strong negative differential resistance (NDR) in the source-drain circuit (Fig.2). Because of the NDR property, RST transistors can be used, e.g., as voltage-controlled oscillators for wireless applications. Efficiency of the RST has been amply demonstrated in III-V heterostructures, where charge injection transitors (CHINT) have demonstrated bandwidths in excess of 100 GHz. Silicon implementations of RST have been so far limited to the Si/GeSi heterosystem.[3] In this paper, I discuss possible implementation of RST transistors in Si, using low-barrier dielectrics, such as zirconium silicates, which are currently under intensive investigation in the context of the low-κ dielectrics program. The SOI technology offers a special advantages both for the implementation of RST devices and their likely application.

While SOI implementation is not essential for the operation of CHINT, its performance will substantially enhanced by higher mobility in the low-doped channel which benefits carrier heating by the applied electric field.

References

[1]A.Kastalsky and S.Luryi, *IEEE Electron Device Lett*. **EDL-4**, 334-336 (1983); S.Luryi et al., *IEEE Trans. Electron Devices* **ED-31**, pp. 832-839 (1984).

[2]G.L. Belenky et al., *Semicond. Sci. Tech.* **9**, 1215-1219 (1994).

[3]M. Mastrapasqua et al., *IEEE Trans. Electron Devices* **ED-43**, 1671-1677 (1996).

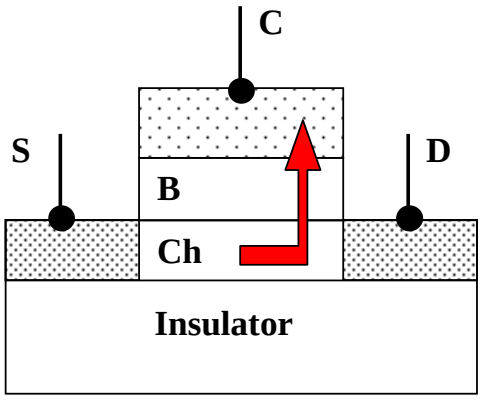

Fig. 1. Schematic diagram of a SOI CHINT. Thin silicon channel (Ch) is confined on side by an insulator and the other by a low-barrier (≈0.5eV) dielectric layer (B). Electrons, heated by an applied S-D field, undergo RST into the collector layer (C). As a result of the RST, the collector current rises while the drain current drops precipitously.

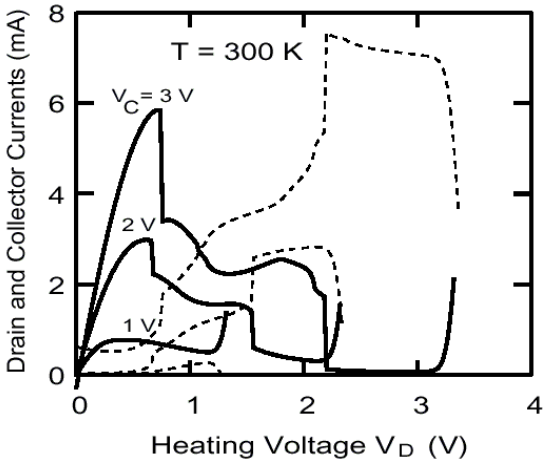

Fig. 2. Family of current-voltage characteristics of a InGaAs/InAlAs CHINT [from P.M. Mensz et al., *Appl. Phys. Lett.* **56**, 2563-2565 (1990)]. Solid lines show current in the channel circuit while dashed lines show the collector current. The barrier height for electron injection in the InGaAs/InAlAs heterojunction lattice matched to InP is about 0.5 eV, which is comparable to that expected at the Si/$(ZrSi)O_2$ interface.