Issues in high performance FinFET and FDSOI transistor design

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The thin-body(TB) structure shown in Fig.1, in FDSOI and FinFET forms, is a relatively new paradigm in transistor design[1-3]. It uses a thin silicon body to obtain good short channel effects (SCEs). As a result heavy body doping is not necessarily needed because better SCEs can be obtained by just making the body thinner. One advantage of the TB approach is that the subthreshold swing can be made virtually ideal, while in the bulk device it is always degraded by the channel to substrate capacitance. A second advantage of the TB structure is it compatible with a silicide metal gate. Silicides have recently been found to be excellent metal gate materials, with low leakage, no mobility degradation, and a simple integration path[4]. The workfunction of the silicides tested so far lies in the middle of the silicon band-gap. This makes silicide gates difficult to use in a bulk devices, but makes them almost ideal for use in TB structures.

Fig. 2 shows the IV characteristics of an NMOS and PMOS FinFET that uses a NiSi as the gate material. The advantage of a metal gate in TB devices is two fold. One, the poly depletion effect is eliminated leading to a larger gate capacitance. Two, the elimination of body doping leads to a lower effective transverse field, increasing mobility by as much as a factor of 2.

The TB structures share some fundamental problems as well. The extension resistance of these structures tends to be a high due to the resistivity of the thin silicon layer. Contact resistance is also a problem due to the lack of silicon for silicidation, this issue can be solved by selectively adding silicon after spacer formation via the raised source/drain(RSD) process. Such a process was utilized in FinFETs shown in Fig. 2.

Although the FinFET and FDSOI devices share many design considerations there are also important distinctions. The advantage of the FDSOI device is its simplicity. Unlike the FinFET it is transparent to the designer, it is also geometrically simpler, and the critical Tsi, silicon body thickness, is defined through a planar process. The disadvantage is in a thinner Tsi required to make the FDSOI device turn off as well as a FinFET. Due to fringing fields in the BOX, the Tsi in FDSOI device has to be more than half as thin as Tsi in a FinFET. As a result the extension resistance is a more significant problem, the fact that resistivity of thin films increases with decreasing thickness due to surface effects only exacerbates the problem further. In addition the thinner Tsi makes quantum confinement effects and surface scattering more pronounced in the FDSOI device.

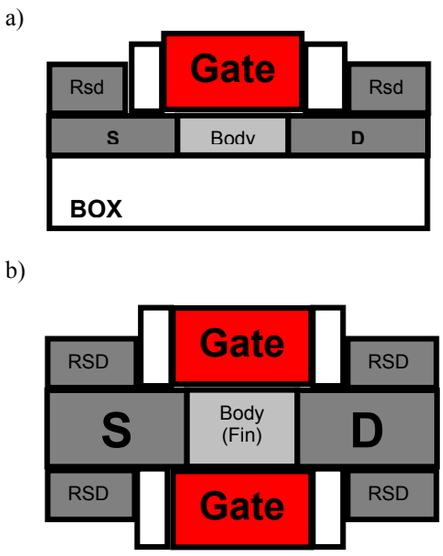

Fig. 1 Electrical structure of thin-body devices (a) in FDSOI single gate form, and (b) in double-gate, for example, FinFET form.

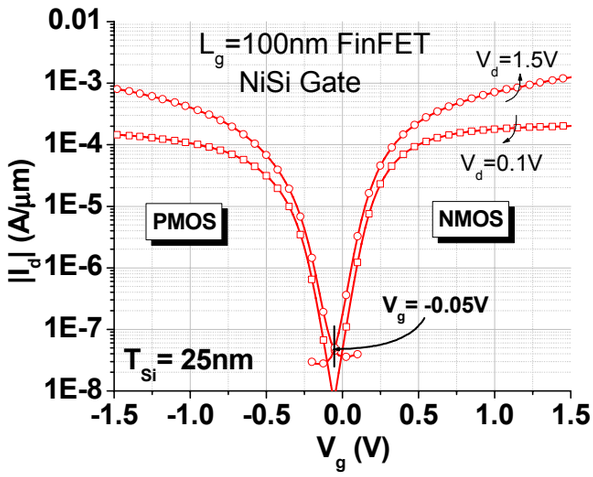

Fig. 2 IV characteristics of a metal gate FinFET. These devices have a NiSi gate, raised source/drain, a 100nm gate length and a 25nm fin thickness.

References:

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