Investigation of Charge Control Related Performances In Double-Gate SOI MOSFETs

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Double-gate SOI MOSFETs are emerging as a key device for future CMOS generations. In this paper, we investigate electrical parameters of major importance for digital and analog performances such as charge-sharing effect (CSE), DIBL, transconductance/drain current ratio (G_m/I_d), output conductance, which are related to the 2D competitive gate vs drain control of the device charge distributions. We studied devices from 3 technologies: 0.25 µm [1], 0.1 µm [2] single gate (SG) fully-depleted (FD) SOI CMOS (for which double-gate operation can be emulated applying a back-gate voltage equal to the front-gate bias multiplied by the ratio of the buried-to-front oxide thicknesses ($k=t_{ox2}/t_{ox1}$)) [3], referred hereafter as quasi double-gate (QDG) and 2 µm FD SOI CMOS in which real double-gate (DG) devices are fabricated using the Gate-all-around (GAA) process [4].

1) We assessed the validity of QDG characterization technique from measurements and 2D device simulations. For the first time it was shown that QDG approach is not valid for weak inversion (WI), while it can be applied to strong inversion (SI) region. Fig. 1 demonstrates that the QDG technique dramatically overestimates the maximum value of G_m/I_d or inverse subthreshold slope (in WI, $S=\ln(10)\cdot(G_m/I_d)^{-1}{}_{max}$) comparing to the real DG device, whereas in SI QDG and real DG are equivalent. For the 0.25 µm and 0.1 µm processes, the value of S in WI for QDG mode was also much lower than 60mV/dec. 2D ATLAS simulations fully support our experimental results and demonstrate that the reason for such difference between WI and SI behaviours lies in potential and carrier distributions (Fig. 2). We then limited the use of QDG regime to gate voltages at least 0.2 V above threshold and verified that process uncertainties which could impair the selection of the proper k ratio by ± 10% do not significantly affect our results.

2) We extracted the V_{th} dependencies on length (i.e. CSE) and drain bias (i.e. DIBL) in SG and QDG operations for transistors with channel lengths, L, from 2 to 0.08 µm on the 0.1 µm process, using techniques based on SI data only. Experimental results for nMOSFETs clearly show that the QDG regime decreases the influence of CSE and DIBL effects (with a factor of 2 to 4) (Fig.3a, b).

3) In 0.1 µm process the saturation currents and transconductances were compared for SG and QDG regimes at constant (V_g-V_{th}) in SI, demonstrating an increase by a factor from 2 to 6 (Fig.3c), which can be related to the volume inversion and higher mobilities. This is also confirmed by the observation on real DG devices (Fig. 1).

4) The output conductance (g_d) in saturation is characterized by the Early voltage ($V_{EA}=I_d/g_d$). Again real DG and QDG devices demonstrate close results, here 4 times better than SG, thanks to the increasing control of the channel by the gate in double-gate regime.

Conclusions: Our results clearly demonstrate the benefits of (even sub-0.1µm) DG over SG devices, not only for digital (S and V_{th} control, drive current), but also analog performances (G_m/I_d, output conductance). We also demonstrated that QDG technique is valid and meaningful with regard to real DG devices in SI only, while in WI it gives a big error.

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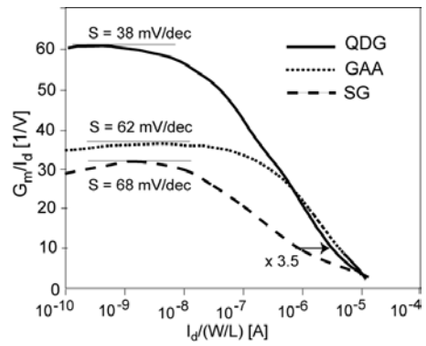

Figure 1. G_m/I_d characteristics for 3 µm QDG, GAA and SG.

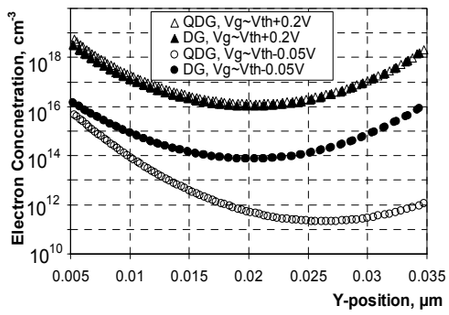

Figure 2. Electron concentration vs Si film depth for DG and QDG cases. Si film and gate oxide thicknesses are 30 nm and 5 nm, respectively; for QDG the buried oxide thickness is 400 nm (i.e. k=80).

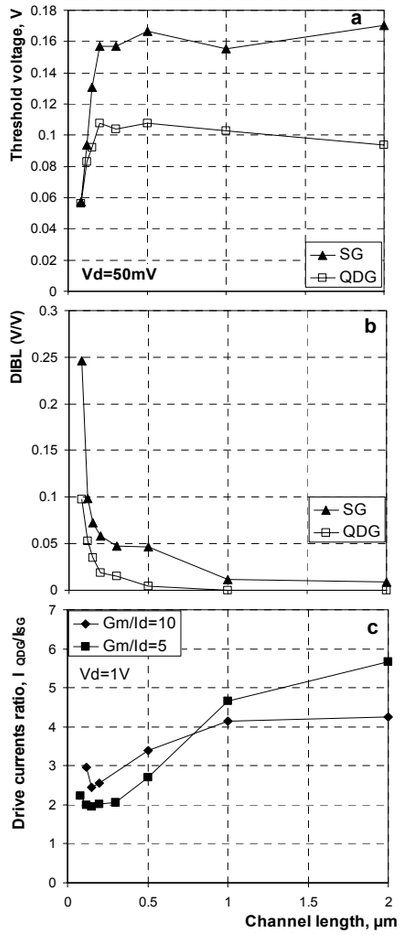

Figure 3. Experimental results of CSE (extracted at (V_d=50 mV)) (a) and DIBL (b) for nMOSFETs in SG and QDG operation regimes. (c) QDG to SG drive currents ratio vs channel length for the same nMOSFETs. Please, note that these transistors were fabricated without HALO's.