Substrate bias effects in SOI FinFETs

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Double-Gate (DG) MOSFETs offer reduced short-channel effects, high mobility and, in general, outperform single-gate devices in terms of performance and scalability. They are expected to sustain the VLSI constraints down to the deca-nanometer range. However, the planar DG technology is rather complex. An attractive solution is to use non-planar transistors such as FinFETs where the process flow is easier to elaborate.

In a FinFET, the gate covers three sides of the body. Most of the carriers are controlled by the two lateral sections of the gate and flow along the body sidewalls. The top section of the transistor is more or less deactivated by using a thicker oxide or nitride. On the other hand, the body is still in contact with the buried oxide (BOX) and substrate related effects are possible.

In this paper, we address for the first time several critical issues: transport properties on the transistor edges, parasitic conduction in the top channel, influence of the substrate bias, and related short-channel and narrow-channel effects. The SOI FinFETs were fabricated at Motorola on a standard Unibond wafer with a 200 nm thick buried oxide and 110 nm film thickness. The channel length and silicon channel thickness (i.e., body width) varied between 10 and 0.08 µm and the silicon channel was left undoped.

Coupling effects. Systematic measurements are presented which show the drain current characteristics, subthreshold swing, transconductance and threshold voltage as a function of the substrate bias. The front channel as well as the two lateral channels are substantially modulated. Basically, the transistor can be operated with two, three, and even four channels (when the substrate is biased in inversion). In depletion, the lateral and front channel coexist. The front channel current depends on the body thickness, whereas the main lateral channels are less affected. In extremely thin bodies, the amount of volume inversion depends on substrate bias. Accumulation at the film-BOX interface can be used to block both the back and the front channels. This allows separating the contributions of the different channels and comparing the carrier mobility at the front, back and lateral interfaces. In addition, our experiments show to what degree the threshold voltage of the FinFETs is substrate bias dependent and can be controlled by a well defined bias or by "back" gate engineering. Another interesting feature is that back-interface accumulation plays the role of a pseudo-ground plane and impacts on the short-channel effects. Numerical simulations are presented which clarify the multiple role of the substrate bias.

Drain current transients. When the substrate is biased in accumulation, necessary majority carriers need to be generated which implies a relatively long process. This results in a time-dependent variation of the drain current. The method of the double-gate drain current transient is adapted to FinFETs for monitoring the carrier lifetime. One variant of this type of measurements consists in maintaining the gate in inversion ($V_G > V_T$), while switching the substrate from depletion to accumulation (or vice-versa). The resulting temporary deficit (or excess) of majority carriers is gradually compensated by carrier generation (or recombination). The results are useful for evaluating the crystal quality of the silicon body and interfaces.

In conclusion, this paper reveals new mechanisms and properties of SOI FinFETs, which are discussed, based on experimental and simulation results. The substrate bias effect on the device characteristics is especially important in terms of interface coupling, threshold voltage control, parasitic front-channel transport, and short-channel effects.