Impact of the Graded-Channel Architecture on Double GateTransistors for High-Performance Analog Applications

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Introduction

The Graded-Channel SOI nMOSFET (GC) is a device that presents an asymmetric channel profile: the natural wafer doping level is kept in the drain side while the threshold voltage ionic implantation is performed in the source side [1] demonstrating significantly enhanced performances [2]. In a first approximation, the device effective channel length is equal to L-L_{LD}, where L is the mask channel length and L_{LD} the length of the low doped region (Fig. 1).

The Gate-All-Around (GAA) nMOSFET is a double gate transistor where the active area (channel) is surrounded by the gate oxide and metal electrode [3], providing excellent analog behavior in high-temperature and radiation hard environments, increasing the Early Voltage (V_{EA}).

In this paper we present, for the first time, the impact of the GC channel architecture on GAA devices, and compare the improvements to those reported from Single-Gate (SG) devices regarding analog circuit design.

Fabrication Process, Measurements and Discussion

Both conventional (uniformly doped from source to drain) and GC GAA transistors have been fabricated according to the process described in [3]. The final thicknesses of the gate oxide, silicon film and buried oxide are 30 nm, 80 nm and 390 nm, respectively. Devices with 3 fingers were made, each one with L=3 µm and W=3 µm (W being the channel width). SG transistors with similar process flow and architecture have also been made for comparison purposes.

In order to evaluate the analog performance of these devices we focused our attention in the low-frequency open-loop gain (A_{V0}) and unity-gain frequency f_T [2]. We can conclude that any increase in A_{V0} is directly related to the improvement in the V_{EA}, up to values of about 1000 V^{-1} dramatically outperforming any previous known 2 to 3 µm long MOSFET. Table 1 indeed compares the extracted V_{EA} and measured I_{DS} for SG and GAA GC transistors. This extraction is performed by linear regression in the range $0.75 \leq V_{DS} \leq 2.0$ V. The same table also presents the V_{EA} extracted from conventional transistors. The GC low doped region causes a modification in the electric field distribution along the channel, reducing the influence of the applied drain bias on the electron concentration of the threshold voltage implanted region, reducing the output conductance (g_D) by about one order of magnitude Due to the extremely improved V_{EA} one can see that the GC GAA can provide very high gain operational amplifiers. The effect of the GAA structure on the device performance can be noted not only in V_{EA} but also in the saturation current, which is about 6 times larger than the similar L_{LD}/L device in SG GC, at the same V_{GT} (V_{GT}=V_{GS}-V_{TH}). Fig. 2 shows I_{DS} against V_{DS}, extracted at V_{GT}=200 mV for all GC GAA nMOSFETs. In GC GAA devices the effect of the channel architecture improves V_{EA} for L_{LD}/L smaller than 0.3. Although for the larger ratios, the impact ionization tends to degrade g_D, the resulting V_{EA} is always larger than in conventional GAA.

Analytical equations and two-dimensional simulations[4] were also used to verify and obtain a better understanding of these devices and the effect of the volume inversion due to the second gate. Table 2 gives a comparison between the simulated results for several studied devices looking to V_{TH} and g_m/I_{DS}. Although for the time being, analytical simulations are only possible for the weak inversion regime, we see that the results are comparable to those obtained from 2D simulations. Similar g_m/I_{DS} results are obtained for conventional and GC GAA. For L_{LD}/L of about 0.83, due to the occurrence of short-channel effects, a small degradation on this parameter is observed.

As a conclusion, we observed that the GC GAA transistor can dramatically increase the intrinsic gain while simultaneously increasing the transconductance, leading to high performance analog circuits outperforming standard MOS devices with these respects.

References

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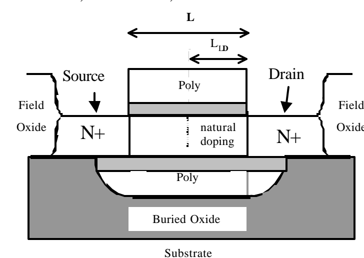

Fig. 1: Cross section of the Graded Channel GAA SOI nMOSFET.

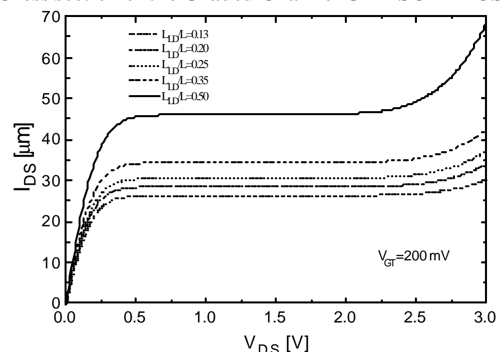

Fig. 2: Measured I_{DS} - V_{DS} curves for the GC GAA.

GC GAA			GC SG		
Mask L_{LD}/L	I_{DS} (µA)	V_{EA}[V]	Mask L_{LD}/L	I_{DS} (µA)	V_{EA}[V]
0.13	26.0	1189	0.08	4.1	41.6
0.20	28.0	988	0.25	5.2	103.7
0.25	30.0	1365	0.32	5.6	164.2
0.35	34.5	816	0.55	8.5	26.7
0.50	45.5	284			
Conventional		150	Conventional		7.5

Table 1: Extracted V_{EA} and measured I_{ds} @ V_{ds}=1.5 V, V_{GT}=200 mV.

GC GAA				
Mask L_{LD}/L	V_{TH} (V)		g_m/I_{DS} (V^{-1})	
	2D simul.	Analytical	2D simul.	Analytical
0	0.24	0.239	38.5	38.6
0.17	0.23	0.229	37.5	38.6
0.33	0.19	0.194	38.0	38.6
0.50	0.19	0.194	38.0	38.6
0.67	0.12	0.120	37.0	38.3
0.83	-0.02	-0.022	30.0	29.5
1.0	-0.30	-0.302	37.9	38.6

Table 2: Simulated and modeled values of V_{TH} and g_m/I_{DS}.